SBC 711
ANALOG INPUT BOARD
HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation, programming information, principles of operation, and service information for the Intel SBC 711 Analog Input board. Additional information is available in the following document: *Intel MULTIBUS Interfacing,* Application Note AP-28.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The SBC 711 Analog Input board is a member of a complete line of Intel SBC 80 system expansion modules. The SBC 711 is a analog input subsystem which, under microprocessor control, performs the basic functions of data acquisition for analog-to-digital conversion. There are three programmable modes of operation for the acquisition of analog inputs: repetitive single channel input, sequential channel scan input, and random channel input.

1-2. DESCRIPTION

The SBC 711 (figure 1-1) is designed to be plugged into a standard SBC 604/614 Modular Backplane and Cardcage to interface directly with an Intel SBC 80 Single Board Computer or used with the Intel Intellec Microcomputer Development System (MDS).

The SBC 711 multiplexer can accommodate 8 differential or 16 single-ended analog input channels. Sockets are provided so that the multiplex capability can optionally be expanded to accommodate an additional 8 differential or 16 single-ended channels by installing two 16-pin dual in-line package (DIP) multiplexers. All input channels are protected to ±28V by clamping diodes and fusible current-limit resistors; this insures the board against potentially destructive overloads under fault conditions.

The differential input channels have provisions for the installation of discrete 250-ohm ±1.0% 1/4W resistors in order to accept 4- to 20-mA current loop inputs. The temperature coefficient of these resistors must be <0.01%/°C.

The selected differential or single-ended input is applied to the analog-to-digital converter (ADC) via a programmable gain amplifier which, under program control, provides gains of 1, 2, 4, or 8. The ADC is a 12-bit, 35.7-microsecond, successive

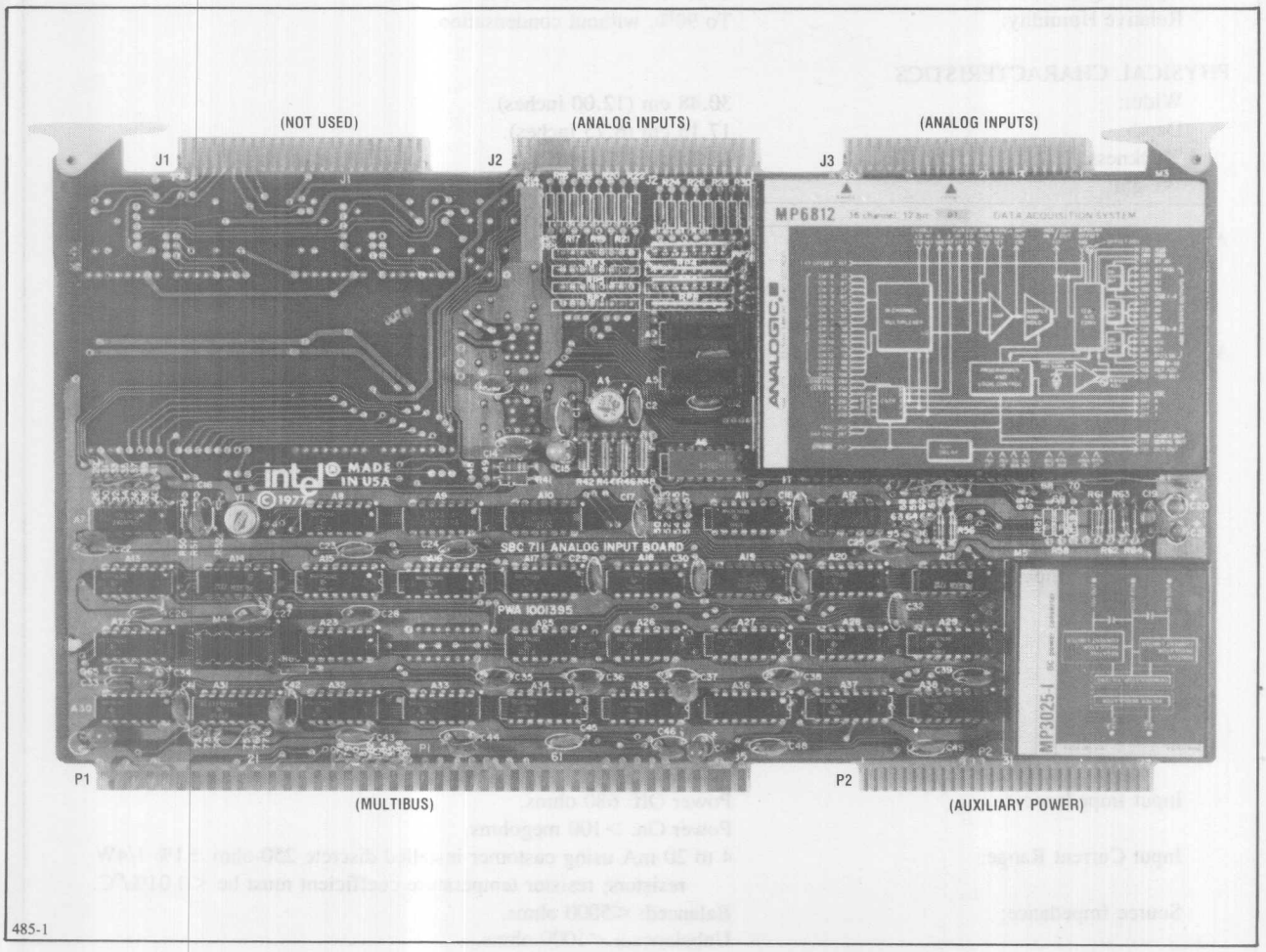


Figure 1-1. SBC 711 Analog Input Board

approximation device with an internal sample-and-hold (S/H) amplifier. The ADC can be jumper-selected for +5V, +10V, ±5V, and ±10V full-scale inputs. The A/D conversion process can be initiated by an external trigger, internal pacer clock, or by programmed command. System interrupts can be generated by (1) end-of-conversion, (2) end-of-scan, or (3) internal pacer clock.

The external trigger is useful when the A/D conversion is to be synchronized to some external event. The internal pacer clock (jumper-selectable intervals from 975 microseconds to 1 second) allows precise, evenly spaced A/D conversions where signal reconstruction is required.

1-3. EQUIPMENT SUPPLIED

The following are supplied with the SBC 711 Analog Input board:

a. Schematic Diagram, dwg no. 2001397
b. Assembly Drawing, dwg no. 1001395

1-4. SPECIFICATIONS

Specifications for the SBC 711 Analog Input board are listed in table 1-1.

Table 1-1. Specifications

POWER REQUIREMENTS: V_{cc} = +5V ±5%.
I_{cc} = 1.7A maximum.

ENVIRONMENTAL REQUIREMENTS
Operating Temperature: 0° to 55°C (32° to 131°F).
Relative Humidity: To 90%, without condensation.

PHYSICAL CHARACTERISTICS
Width: 30.48 cm (12.00 inches).
Depth: 17.15 cm (6.75 inches).
Thickness: 1.27 cm (0.50 inch).
Weight: 454 gm (16 ounces).

ADDRESSING: Reserves a block of 16 contiguous memory locations relative to a jumper-selectable memory base address. Programming information is provided in Chapter 3.

ANALOG INPUT
Number of Channels: 8 differential or 16 single-ended; expandable to 16 differential or 32 single-ended using two plug-in 8:1 multiplexers (Harris H1818A or equivalent).
Resolution: 12-bits (0.025%), bipolar or unipolar.
S/H Aperture Time: <20 nanoseconds.
S/H Uncertainty: 5 nanoseconds.

Multiplexer Input Voltage Ranges:

Gain X	A/D Input Range				
	+5V	+10V	±5V	±10V	Jumper Selectable
1	+5V	+10V	±5V	±10V	Programmable
2	+2.5V	+5V	±2.5V	±5V	
4	1.25V	+2.5V	±1.25V	±2.5V	
8	0.625V	+1.25V	±0.625V	±1.25V	

Input Impedance: Power Off: 680 ohms.
Power On: >100 megohms.
Input Current Range: 4 to 20 mA using customer-installed discrete 250-ohm ±1% 1/4W resistors; resistor temperature coefficient must be <0.01%/°C.
Source Impedance: Balanced: <5000 ohms.
Unbalanced: <1000 ohms.

Table 1-1. Specifications (Continued)

Common Mode Rejection (CMR):	60 dB (differential input).
Common Mode Voltage (CMV):	±10.24V (signal plus common mode).
Input Overvoltage Protection:	±28V (dc); 28V peak ac.
Overall Accuracy (25°C):	0.05% FSR ±1/2 LSB (gain X1). 0.07% FSR ±1/2 LSB (gain X2, X4, X8). (Includes 3σ noise, linearity, offset gain, and dynamic response errors.)
Temperature Coefficient:	0.0025% FSR/°C (Gain X1). 0.0030% FSR/°C (Gain X2, X4, X8).
A/D Conversion Speed:	28 kHz.
THROUGHPUT*	
Sample Rate (Single Channel):	17 kHz.
Channel-to-Channel Rate:	16 kHz.
EXTERNAL TRIGGER:	TTL compatible; 1.5 μsec (minimum) pulse width, better than 50 nsec rise time.
INTERNAL PACER CLOCK:	Crystal-controlled accuracy 0.05%; divider provides range of $\frac{1000}{2^n}$ msec where n = 0 through 10.

INTERFACE CONNECTORS:

Interface	No. of Pins	Pin Centers in.	Pin Centers mm	Mating Connectors
P1 Multibus	86	0.156	3.96	CDC VPB01E43A00A1
P2 ±15V Aux Power	60	0.1	2.54	CDC VPB01B30A00A2 TI H3-11130
J2 1st 8/16 Input Channels	50	0.1	2.54	3M 3415-0000 or T1 H3-12125
J3 Expander 8/16 Input Channels	50	0.1	2.54	Same as J2

*Assuming 2-MHz CPU clock. Includes time required to transfer data from the SBC 711 to system memory.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the SBC 711 Analog Input board. These instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, and bus interface requirements; jumper configurations; optional auxiliary power connections; multiplexer channel expansion; current loop input resistor installation; analog input cabling; and board installation.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support center (see paragraph 5-10) to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The SBC 711 is designed for interface with an Intel SBC 80 Single Board Computer based system or an Intel Intellec Microcomputer Development System (MDS). Important installation and interfacing criteria are presented in following paragraphs.

2-4. POWER REQUIREMENT

The SBC 711 requires +5V (±0.25V) at 1.7A maximum. For installation in an SBC 80 Single Board Computer based system, ensure that the system power supply has sufficient +5V current overhead to accommodate the additional requirement. For installation in an Intellec MDS, calculate the total +5V current requirement for the standard modules and all installed optional modules. Ensure that the additional 1.7A (maximum) current requirement will not exceed the capacity of the +5V supply.

2-5. COOLING REQUIREMENT

The SBC 711 dissipates 121 gram-calories/minute (0.49 Btu/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The system 80 enclosures and the Intellec MDS include fans to provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the SBC 711 are as follows:

a. Width:	30.48 cm (12.00 inches)
b. Height:	17.15 cm (6.75 inches)
c. Thickness:	1.27 cm (0.50 inch)

2-7. BUS INTERFACE REQUIREMENTS

The SBC 711 is designed for installation in a standard Intel SBC 604/614 Modular Backplane and Cardcage or in the Intellec MDS motherboard. As shown in figure 1-1, edge connector P1 provides interface to the Multibus. Connector P1 pin assignments are listed in table 2-1 and descriptions of the signal functions are given in table 2-2; an alternative mating connector for P1 is specified in table 1-1. Edge connector P2 is an auxiliary power input/output connector as described in paragraph 2-15.

The ac and dc characteristics of the SBC 711 are presented in tables 2-3 and 2-4, respectively. The bus exchange timing for memory read and write operations is shown in figure 2-1.

2-8. JUMPER CONFIGURATIONS

Instruction for configuring jumpers for various control functions of the SBC 711 are provided in following paragraphs.

Table 2-1. Multibus Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44	ADRF/	Address bus
2	GND		45	ADRC/	
3	+5 VDC	Power input	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7			50	ADR9/	
8			51	ADR6/	
9			52	ADR7/	
10			53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13			56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15			58	ADR1/	
16			59		
17			60		
18			61		
19	MRDC/	Memory Read Command	62		
20	MWTC/	Memory Write Command	63		
21			64		
22			65		
23	XACK/	Transfer Acknowledge	66		
24	INH1/	Inhibit RAM	67	DAT6/	Data bus
25			68	DAT7/	
26	INH2/	Inhibit ROM	69	DAT4/	
27			70	DAT5/	
28			71	DAT2/	
29			72	DAT3/	
30			73	DAT0/	
31	CCLK/	Constant Clock	74	DAT1/	
32			75	GND	Ground
33			76	GND	
34			77		
35	INT6/	Interrupt request on level 6	78		
36	INT7/	Interrupt request on level 7	79		
37	INT4/	Interrupt request on level 4	80		
38	INT5/	Interrupt request on level 5	81	+5 VDC	Power input
39	INT2/	Interrupt request on level 2	82	+5 VDC	
40	INT3/	Interrupt request on level 3	83	+5 VDC	
41	INT0/	Interrupt request on level 0	84	+5 VDC	
42	INT1/	Interrupt request on level 1	85	GND	Ground
43	ADRE/		86	GND	

*All unassigned pins are reserved.

Table 2-2. Multibus Signal Functions

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0/-ADRF/	*Address*. These 16 lines transmit the address of the ADC and various registers on the SBC 711. ADRF/ is the most significant bit.
CCLK/	*Constant Clock*. A clock signal of constant frequency supplied by the system controller. The frequency, period, and duty cycle of CCLK/ depends on which controller is employed.
DAT0/-DAT7/	*Data*. These eight bidirectional lines transmit and receive data to and from the addressed register on the SBC 711.
INIT/	*Initialize*. Clears certain registers on the SBC 711.
INH1/	*Inhibit RAM*. Generated when the SBC 711 is addressed to prevent any RAM sharing the same address from responding.
INH2/	*Inhibit ROM*. Generated when the SBC 711 is addressed to prevent any ROM (or PROM) sharing the same address from responding.
INT0/-INT7/	*Interrupt*. These eight lines input interrupt requests to the system controller. INT0/ has the highest priority and INT7/ has the lowest priority.
MRDC/	*Memory Read Command*. Indicates that the address of the SBC 711 is on the Multibus address lines and that the output of the addressed register is to be read (placed) onto the Multibus data lines.
MWTC/	*Memory Write Command*. Indicates that the address of the SBC 711 is on the Multibus address lines and that the contents on the Multibus data lines are to be loaded into the addressed register.
XACK/	*Transfer Acknowledge*. Indicates that the SBC 711 has completed the specified Memory Read or Memory Write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 2-3. SBC 711 AC Characteristics

PARAMETER	MIMIMUM (nsec)	MAXIMUM (nsec)	DESCRIPTION	REMARKS
t_{AS}	50		Address Setup to Command	
t_{DS}	50		Write Data Setup to Command	
*t_{XACK}	50	1500	Command to Transfer Acknowledge	Jumper selectable. See paragraph 2-14.
t_{WCMD}	100		Write Command Pulse Width	
t_{AH}	50		Address Hold Time	
t_{DH}	50		Write Data Hold Time	
t_{DHR}	0		Read Data Hold Time	
t_{TO}		65	Acknowledge Turn Off Delay	
t_{ACC}		200	Access Time to Read Data	
t_{RCMD}	250		Read Command Pulse Width	
t_{CCLK}	100		Constant Clock	From system controller

*Assuming a CCLK frequency of 9.216 MHz.

Table 2-4. SBC 711 DC Characteristics

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN.	MAX.	UNITS
ADR0/-ADRF/ MRDC/ MWTC/	V_{IL} V_{IH} I_{IL} I_{IH} *C_L	Input Low Voltage Input High Voltage Input Current at Low V Input Current at High V Capacitive Load	 V_{IN} = 0.4 V_{IN} = 2.7	 2.0	0.8 −0.4 20 18	V V mA μA pF
XACK/	V_{OL} V_{OH} I_{LH} I_{LL} *C_L	Output Low Voltage Output High Voltage Output Leakage High Output Leakage Low Capacitive Load	I_{OL} = 32 mA I_{OH} = −5.2 mA V_O = 2.4 V_O = 0.4	 2.4	0.4 40 −40 15	V V μA μA pF
DAT0/-DAT7/	V_{OL} V_{OH} V_{IL} V_{IH} I_{IL} I_{LH} *C_L	Output Low Voltage Output High Voltage Input Low Voltage Input High Voltage Input Current at Low V Output Leakage High Capacitive Load	I_{OL} = 55 mA I_{OH} = −10 mA V_{IN} = 0.45 V_O = 5.25	 2.4 2.0	0.6 0.95 −0.25 100 18	V V V V mA μA pF
INIT/	V_{IL} V_{IH} I_{IL} I_{IH} *C_L	Input Low Voltage Input High Voltage Input Current at Low V Input Current at High V Capacitive Load	 V_{IN} = 0.4 V_{IN} = 2.4	 2.0	0.8 −1.6 400 18	V V mA μA pF
INH1/-INH2/ INT0/-INT7/	V_{OL} V_{OH} V_{IL} V_{IH} I_{IL} I_{IL} *C_L	Output Low Voltage Output High Voltage Input Low Voltage Input High Voltage Input Current at Low V Input Current at High V Capacitive Load	I_{OL} = 16 mA OPEN COLLECTOR V_{IN} = 0.4 V_{IN} = 2.4	 2.0	0.4 0.8 −1.6 400 22	V V V mA μA pF

*Capacitance values are approximations.

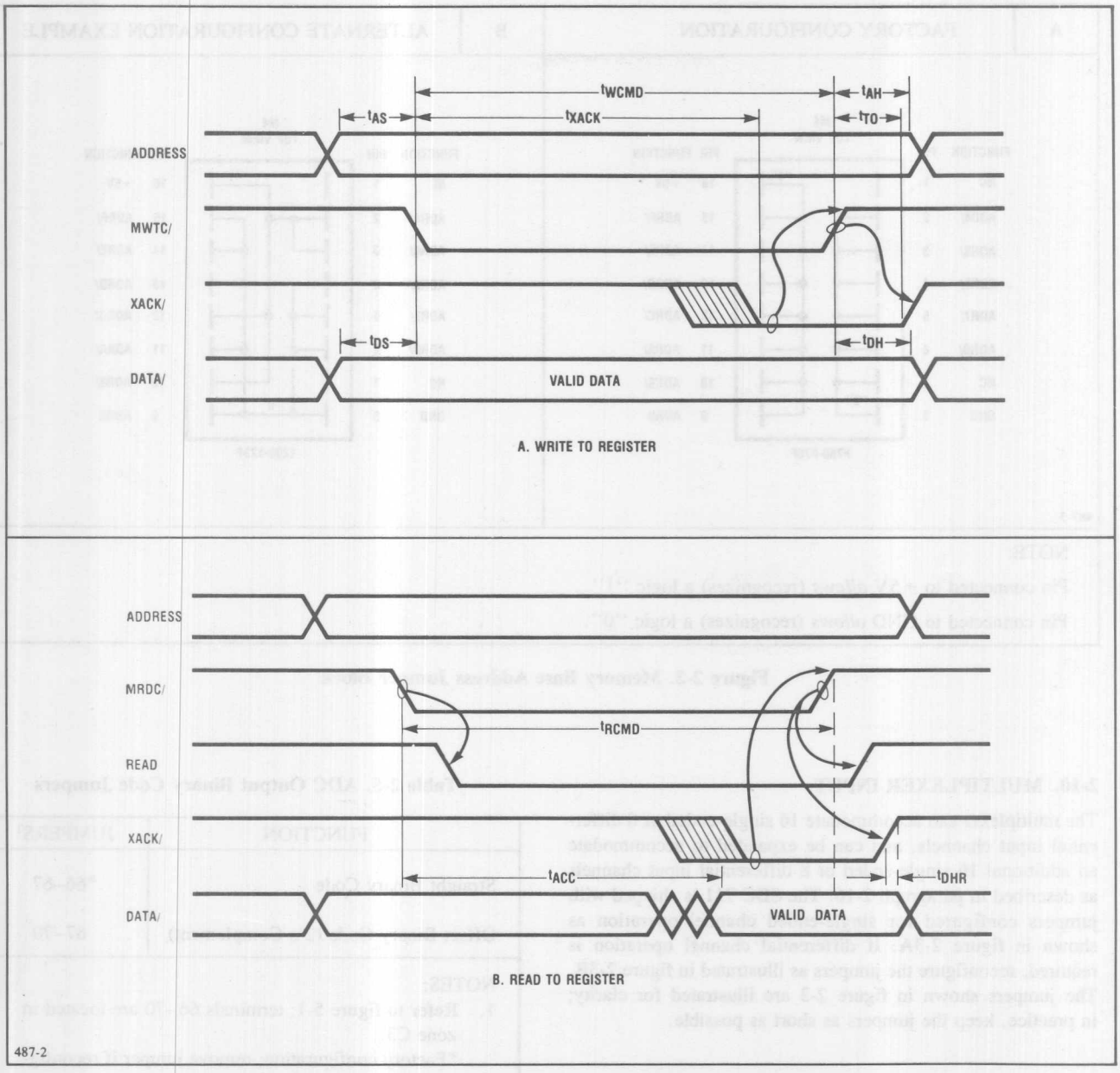


Figure 2-1. Bus Exchange Timing

2-9. MEMORY BASE ADDRESS

The system processor communicates with the SBC 711 by issuing Memory Read and Memory Write commands. The memory addresses used for these commands are relative to a 16-bit base address that must lie on a 16-byte boundary; this memory base address is assigned by the user by means of jumper wires installed in a 16-pin DIP header. The header is then installed in IC socket M4 as shown in figure 5-1 zone B7.

The 16-pin DIP header is configured at the factory for memory base address F700; i.e., the SBC 711 will recognize memory addresses F700-F70F. Figure 2-2 shows two examples of how to configure the desired memory base address. Figure 2-2A shows the jumpers as configured at the factory; figure 2-2B shows as an example how to configure the jumpers for a memory base address of 1230. Note that each of the address bits ADRF/-ADR4/ must be jumpered either to GND or +5V.

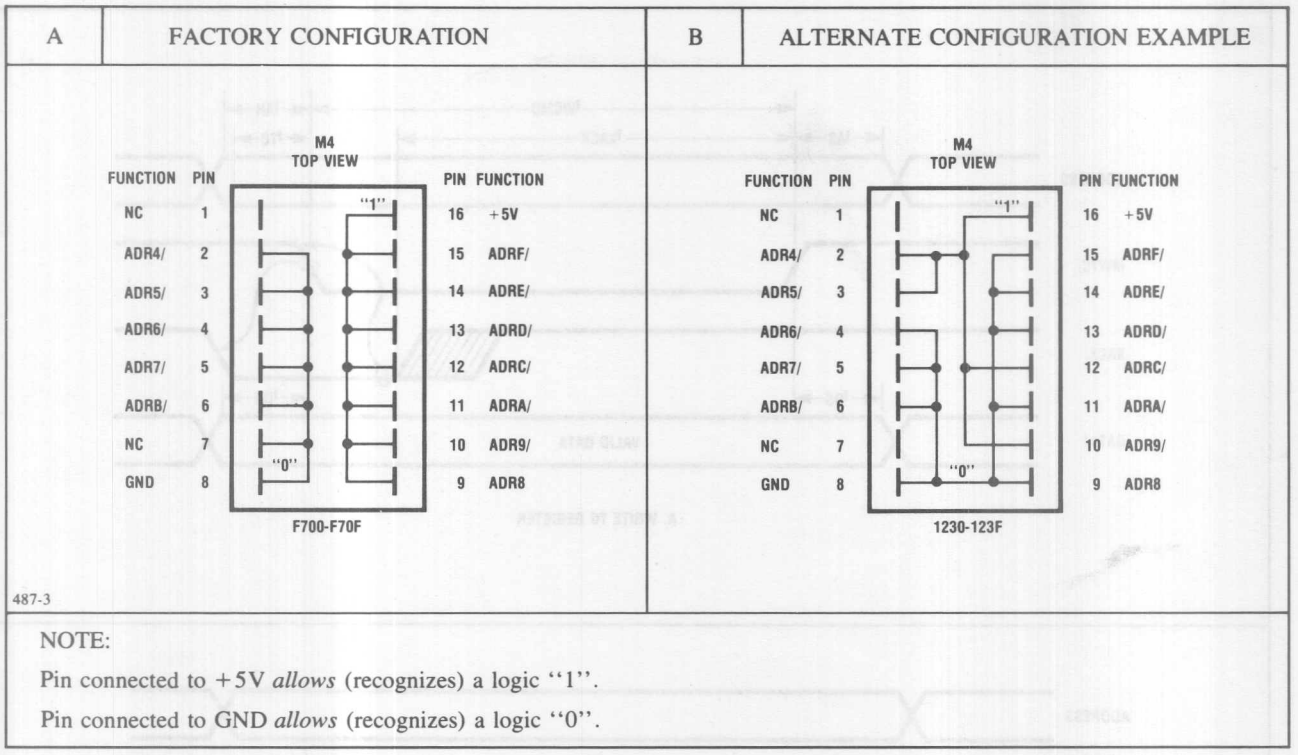


Figure 2-2. Memory Base Address Jumper Block

2-10. MULTIPLEXER INPUT

The multiplexer can accommodate 16 single-ended or 8 differential input channels, and can be expanded to accommodate an additional 16 single-ended or 8 differential input channels as described in paragraph 2-16. The SBC 711 is shipped with jumpers configured for single-ended channel operation as shown in figure 2-3A. If differential channel operation is required, reconfigure the jumpers as illustrated in figure 2-3B. The jumpers shown in figure 2-3 are illustrated for clarity; in practice, keep the jumpers as short as possible.

2-11. ADC CONFIGURATION

The ADC is configured at the factory to convert the analog input voltage to a straight binary coded output. If an offset binary-coded output is desired, reconfigure the jumpers as listed in table 2-5.

Table 2-6 lists the jumpers required to select the desired full-scale input voltage range and polarization. As indicated in table 2-6, the ADC is configured at the factory for ±10V full-scale voltage operation. The ADC should be recalibrated each time it is reconfigured for a different full scale voltage range. (Refer to Chapter 5.)

If the current range is used, precision resistors must be installed as described in paragraph 2-17. Also if the current range is used, the multiplexer input must be configured for differential channel operation as described in paragraph 2-10.

Table 2-5. ADC Output Binary Code Jumpers

FUNCTION	JUMPERS[1]
Straight Binary Code	*66–67
Offset Binary Code (2's Complement)	67–70

NOTES:
1. Refer to figure 5-1; terminals 66–70 are located in zone C3.
*Factory configuration; remove jumper if reconfiguring for offset binary code.

2-12. ADC TRIGGER

A trigger pulse (TADC/), which is required to start the A/D conversion at precise intervals, may be obtained from the on-board pacer clock or from an external TADC/ clock. If the on-board pacer clock is used, select and jumper the desired TADC/ clock rate as listed in table 2-7. If more precise timing is required than supplied by the on-board pacer clock, an external TADC/ clock may be input via pin 42 of connector J2. Figure 2-4 provides the external TADC/ clock characteristics and jumper connections.

Table 2-6. ADC Range and Polarization Jumpers

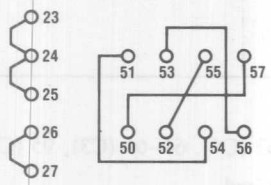
FULL-SCALE VOLTAGE RANGE[1]				FULL-SCALE CURRENT RANGE[2]
+5V	+10V	±5V	±10V	4–20 mA
JUMPERS[3]				JUMPERS[3]
58–59 60–61	58–71 60–61	58–71 60–62	*58–71 *60–62	58–59 60–61

NOTES:

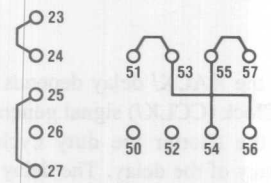
1. Configure multiplexer jumpers as required for single-ended or differential channel operation; refer to paragraph 2-10.
2. Configure multiplexer jumpers for differential channel operation; refer to paragraph 2-10.
3. Refer to figure 5-1. Terminals 58 through 62 are located in zones C4, C3; terminal 71 is located in zone C2.

*Factory configuration; remove jumpers if reconfiguring for a different voltage range or for current range.

A	SINGLE-ENDED CHANNELS



B	DIFFERENTIAL CHANNELS



487-4

NOTE:

Refer to figure 5-1. Terminals 23 through 27 are located in zone C4; terminals 51 through 57 are located in zone B5.

Figure 2-3. Multiplexer Input Selection Jumpers

2-13. INTERRUPTS

The SBC 732 provides two jumper selectable interrupts which may be interfaced to the system computer via the Multibus. Select interrupt "A" and/or interrupt "B" by connecting the jumpers as specified in table 2-8.

After interrupt "A" and/or Interrupt "B" jumpers have been connected, these interrupts can be individually connected to separate Multibus interrupt lines or OR-tied to one Multibus interrupt line. (Refer to table 2-9.) To connect Interrupt "A" to Multibus INT7/, for example, connect a jumper between terminals 78 and 81; to OR-tie *both* Interrupt "A" and "B" to Multibus INT3/, connect a jumper between terminals 78, 79, and 85.

2-14. TRANSFER ACKNOWLEDGE DELAY

The SBC 711 generates a Transfer Acknowledge (XACK/) signal in response to Memory Read and Memory Write Commands from the system computer. As listed in table 2-10, the XACK/ response from the SBC 711 may be delayed for 50 nanoseconds to 1.5 microseconds after the receipt of a command in order to ensure compatability with the system computer timing. (Refer to paragraphs 4-11 and 4-12.)

Table 2-7. Internal TADC/ Clock Rate Jumper

CLOCK RATE	JUMPER[1]
1.000 sec	40–28
500.0 msec	40–31
250.0 msec	40–30
62.50 msec	40–33
31.25 msec	40–32
15.63 msec	40–35
7.813 msec	40–34
3.906 msec	40–37
1.953 msec	40–36
976.6 μsec	*40–38

NOTES:

1. Terminals are located in figure 5-1 zone C7.

*Factory configuration; remove jumper if reconfiguring for different clock rate.

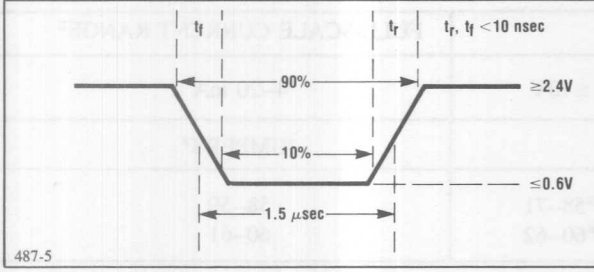
CHARACTERISTICS	JUMPERS[1]
	39–40 48–49*
	NOTE: 1. Refer to figure 5-1. Terminals 39 and 40 are located in zone C7; terminals 48 and 49 are located in zone C6. *Factory configuration.

Figure 2-4. External TADC/ Clock Characteristics and Jumpers

Table 2-8. Board Interrupt Jumpers

INTERRUPT "A"			INTERRUPT "B"		
PACER	EOC	EOS	PACER	EOC	EOS
JUMPER[1]			JUMPER[1]		
63–64 **41–32	64–96	*64–65	63–95 **41–32	*95–96	65–95

NOTES:

1. Refer to figure 5-1; terminals are located in the following zones: 41 (C7), 63 (C4), 64–65 (C3), 95 (C4), 96 (C3).

*Factory configuration; remove appropriate jumper if reconfiguration is required.

**Pacer interrupt factory set to 31.25 msec. If different interval is desired, disconnect jumper 41–32 and jumper terminal 41 to appropriate clock rate jumper listed in table 2-7.

Table 2-9. Multibus Interrupt Jumpers

	FUNCTION	TERMINAL[1]
SBC 711	Interrupt "A" Interrupt "B"	78 79
MULTIBUS	INT0/ INT1/ INT2/ INT3/ INT4/ INT5/ INT6/ INT7/	86 87 84 85 82 83 80 81

NOTE:

1. Refer to figure 5-1; terminals 78 through 87 are located in zone B6.

The tolerance of the XACK/ delay depends on the duty cycle of the Constant Clock (CCLK/) signal generated by the system computer; i.e., the shorter the duty cycle of CCLK/, the greater the accuracy of the delay. The delay timer is advanced on the leading edge of CCLK/, and XACK/ is generated on the trailing edge of CCLK/.

Terminals 72, 73, 77, and 76 must each be connected to either terminal 74 or 75. For instance, to enforce a delay of 1.0 microsecond, jumper terminals 73 and 76 to terminal 74; jumper terminals 72 and 77 to terminal 75. (Refer to table 2-10.)

2-15. AUXILIARY POWER (SPECIAL)

The SBC 711 includes a dc-to-dc converter module (M5) which supplies +15V and −15V power at 150 mA to the analog circuits. In some special applications the user may wish to power an external function from this converter or remove the converter and power the SBC 711 analog circuits from an external regulated source. Table 2-11 lists the factory installed jumpers to accommodate auxiliary power inputs or outputs.

Table 2-10. Transfer Acknowledge Delay Jumpers

JUMPERS[1]				DELAY (TYP)
72	73	77	76	(μsec)
74	74	74	74	*0.05
74	74	74	75	0.1
74	74	75	74	0.2
74	74	75	75	0.3
74	75	74	74	0.4
74	75	74	75	0.5
74	75	75	74	0.6
74	75	75	75	0.7
75	74	74	74	0.8
75	74	74	75	0.9
75	74	75	74	1.0
75	74	75	75	1.1
75	75	74	74	1.2
75	75	74	75	1.3
75	75	75	74	1.4
75	75	75	75	1.5

NOTES:

1. Refer to figure 5-1; terminals 72 through 77 are located in zone B7.

*Factory configuration; remove jumpers if reconfiguring for different delay.

Auxiliary power is input or output via edge connector P2. Pin assignments are listed in table 2-12 and the required mating connector is specified in table 1-1 (Specifications). Install the mating connector for P2 in line with the backplane mating connector for P1. (See figure 1-1.)

Table 2-11. Auxiliary Power Jumpers

FUNCTION	JUMPER[1]
+15V	*90–91
−15V	*92–93
Analog Return/Auxiliary Power Common	*88–89

NOTE:

1. Refer to figure 5-1; terminals 88 through 93 are located in zone B2.

*Jumpers are factory installed.

2-16. MULTIPLEXER CHANNEL EXPANSION

The SBC 711 can be expanded by an additional 16 single-ended or 8 differential input channels by installing two Harris H1818A 8:1 Multiplexers. Install the multiplexers in IC sockets A2 and A5. Refer to figure 5-1 zone C4. Orient the multiplexer IC's with the notched ends (pin 1) facing in the same direction as the other IC's on the board.

2-17. CURRENT LOOP INPUT RESISTORS

The SBC 711 can be adapted to accept 4- to 20-mA current loop inputs by the installation of discrete 250-ohm ±1% 1/4W resistors; one discrete resistor is required for each channel. Refer to table 2-13 and install a resistor(s) in the appropriate channel(s). It should be noted that the ADC must be operated in the differential input mode for current loop applications.

Table 2-12. Auxiliary Power Connector P2 Pin Assignments

PIN*	FUNCTION	PIN*	FUNCTION
21	Analog Return/Aux Pwr Common	22	Analog Return/Aux Pwr Common
23	+15V	24	+15V
25	−15V	26	−15V

NOTE:

All odd-numbered pins (1, 3,. . . 59) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the board extractors at the top.

*Unlisted pins are reserved for future use.

Table. 2-13. Current Loop Input Resistors

DIFF CHAN	RESISTOR[1]	DIFF[2] CHAN	RESISTOR[1]
0	R22	8	R30
1	R21	9	R29
2	R20	10	R28
3	R19	11	R27
4	R18	12	R26
5	R17	13	R25
6	R16	14	R24
7	R15	15	R23

NOTES:

1. Refer to figure 5-1. R15 through R22 are located in zone D5; R23 through R30 are located in zone D4.
2. Channels 8–15 available only when H1818A multiplexers are installed. See paragraph 2-16.

2-18. ANALOG INPUT CABLING

Connector J2 provides the interface between the 8 standard differential analog channels (CH 0 through CH 7) or 16 single-ended channels (CH 0 through CH 15). Refer to table 2-14.

Connector J3 provides the interface between the 8 user-expanded differential channels (CH 8 through CH 15) or 16 single-ended channels (CH 16 through CH 31). Refer to table 2-15.

Figures 2-5 and 2-6 illustrate methods of connecting single-ended and differential voltage sources to the SBC 711 inputs. Figure 2-7 shows single-ended sources connected as differential inputs to eliminate ground loops and thereby reduce the common-mode voltage. Figure 2-8 illustrates the method of connecting current source inputs.

Table 2-14. Analog Input Connector J2 Pin Assignments

PIN	SINGLE-ENDED	DIFFERENTIAL	PIN	SINGLE-ENDED	DIFFERENTIAL
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Analog Return	4	CH 0	CH 0 HI
5	↕	↕	6	CH 8	CH 0 LO
7			8	CH 1	CH 1 HI
9			10	CH 9	CH 1 LO
11			12	CH 2	CH 2 HI
13			14	CH 10	CH 2 LO
15			16	CH 3	CH 3 HI
17			18	CH 11	CH 3 LO
19			20	CH 4	CH 4 HI
21			22	CH 12	CH 4 LO
23			24	CH 5	CH 5 HI
25			26	CH 13	CH 5 LO
27			28	CH 6	CH 6 HI
29			30	CH 14	CH 6 LO
31	↕	↕	32	CH 7	CH 7 HI
33	Analog Return	Analog Return	34	CH 15	CH 7 LO
35	Not Used	Not Used	36	Not Used	Not Used
37	Not Used	Not Used	38	Not Used	Not Used
39	Digital Common	Digital Common	40	Clock Out	Clock Out
41	↕	↕	42	Ext. Trigger In	Ext. Trigger In
43			44	EOC Status Out	EOC Status Out
45	Digital Common	Digital Common	46	EOS Status Out	EOS Status Out
47	Analog Return	Analog Return	48	Analog Return	Analog Return
49	−15V	−15V	50	+15V	+15V

NOTE:

All odd-numbered pins (1, 3, . . . 49) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

Table 2-15. Analog Input Connector J3 Pin Assignments

PIN	SINGLE-ENDED	DIFFERENTIAL	PIN	SINGLE-ENDED	DIFFERENTIAL
1	Not Used	Not Used	2	Not Used	Not Used
3	Analog Return	Analog Return	4	CH 16	CH 8 HI
5			6	CH 24	CH 8 LO
7			8	CH 17	CH 9 HI
9			10	CH 25	CH 9 LO
11			12	CH 18	CH 10 HI
13			14	CH 26	CH 10 LO
15			16	CH 19	CH 11 HI
17			18	CH 27	CH 11 LO
19			20	CH 20	CH 12 HI
21			22	CH 28	CH 12 LO
23			24	CH 21	CH 13 HI
25			26	CH 29	CH 13 LO
27			28	CH 22	CH 14 HI
29			30	CH 30	CH 14 LO
31			32	CH 23	CH 15 HI
33	Analog Return	Analog Return	34	CH 31	CH 15 LO
35	Not Used	Not Used	36	Not Used	Not Used
37			38		
39			40		
41			42		
43			44		
45	Not Used	Not Used	46	Not Used	Not Used
47	Analog Return	Analog Return	48	Analog Return	Not Used
49	−15V	−15V	50	+15V	+15V

NOTE:
All odd-numbered pins (1, 3, . . . 49) are on component side of the board. Pin 1 is the right-most pin when viewed from the component side with the board extractors at the top.

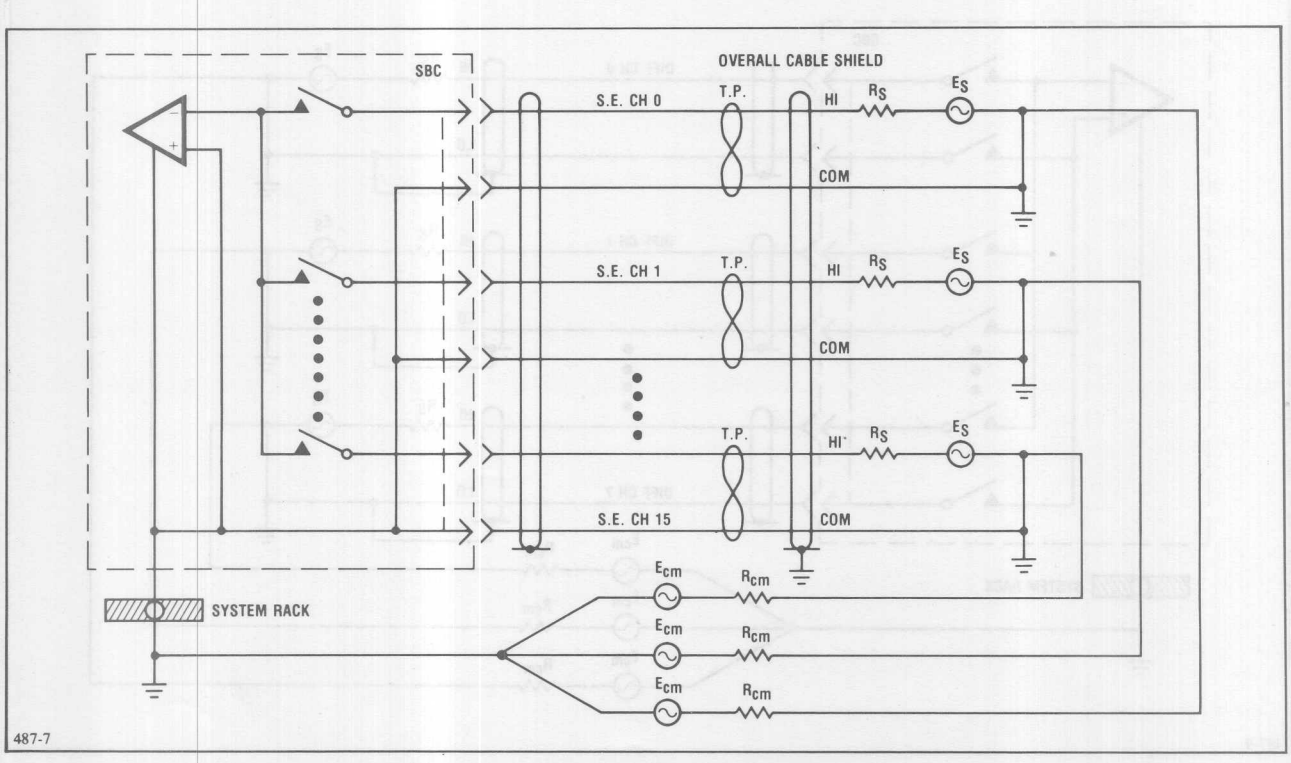


Figure 2-5. Single-Ended Analog Input Cabling

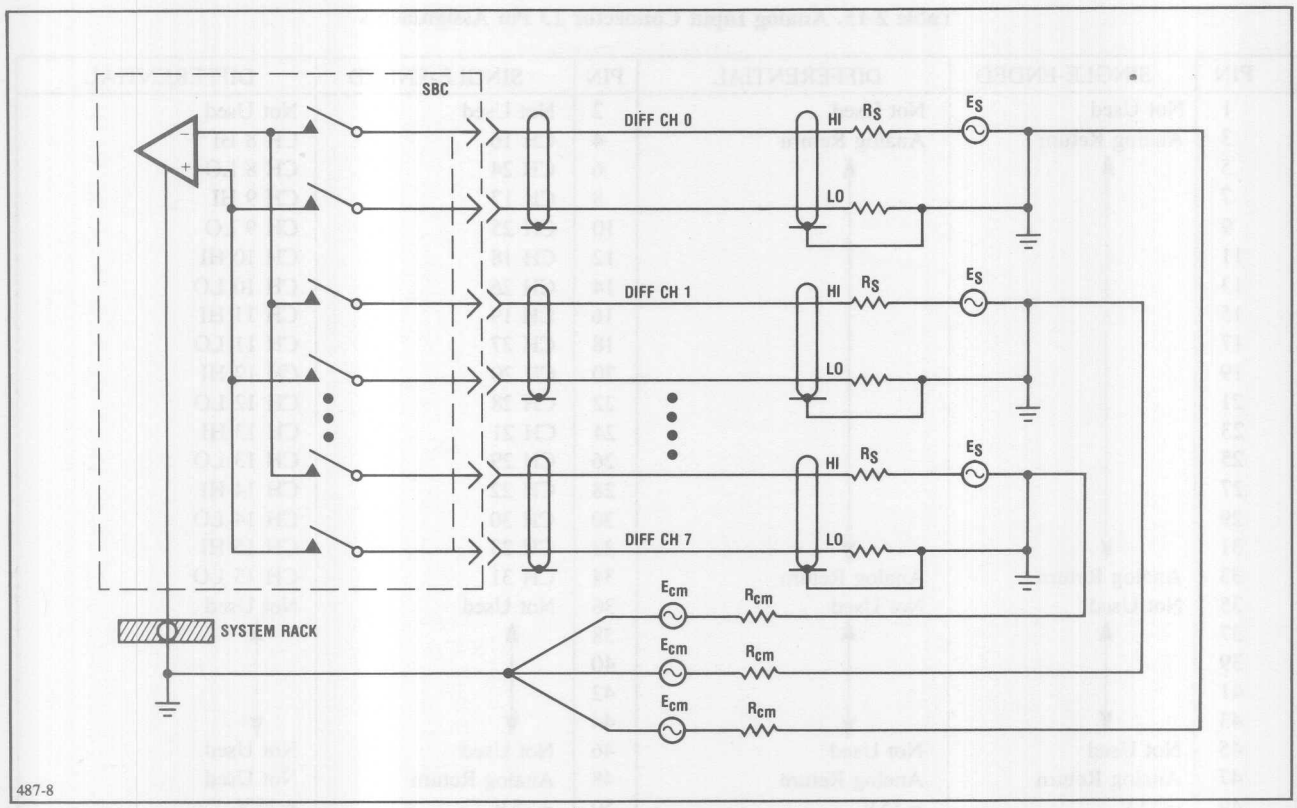


Figure 2-6. Differential Analog Input Cabling (Differential Sources)

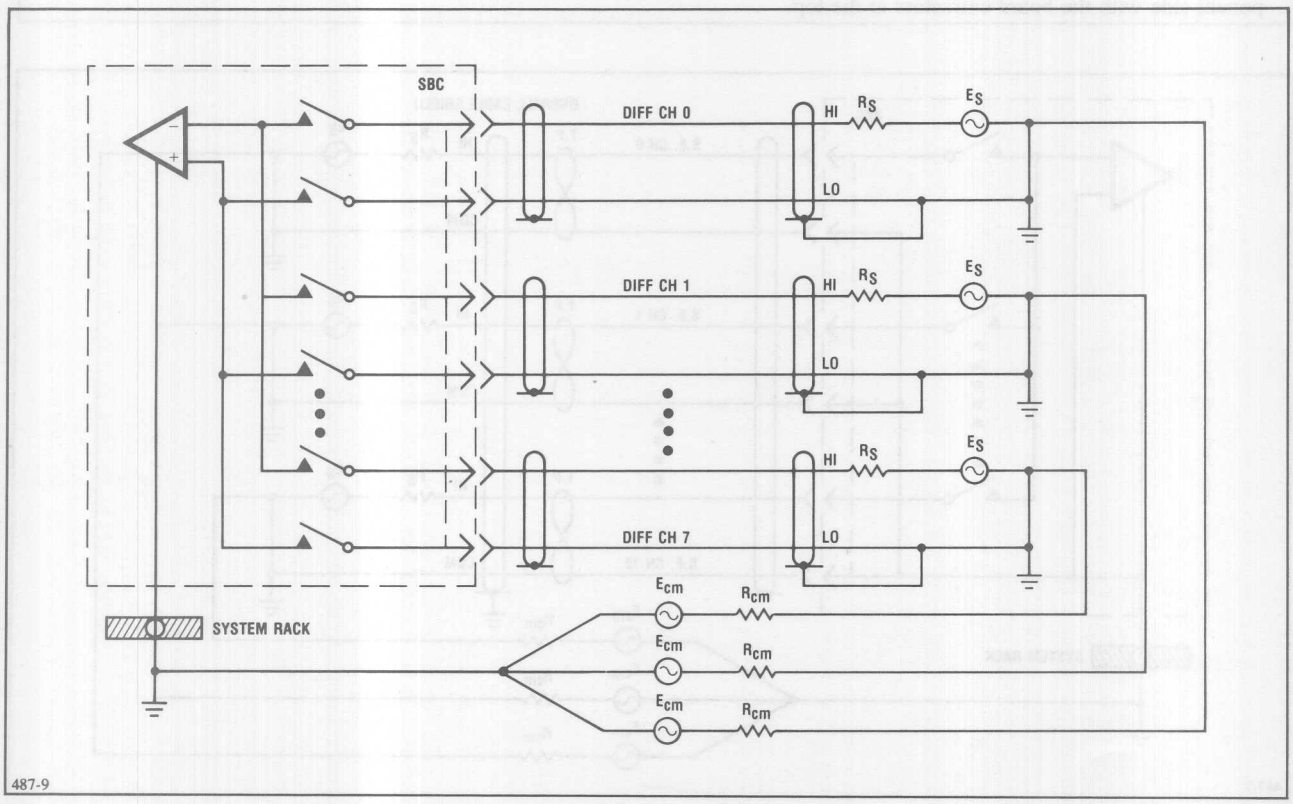


Figure 2-7. Differential Analog Input Cabling (Single-Ended Sources)

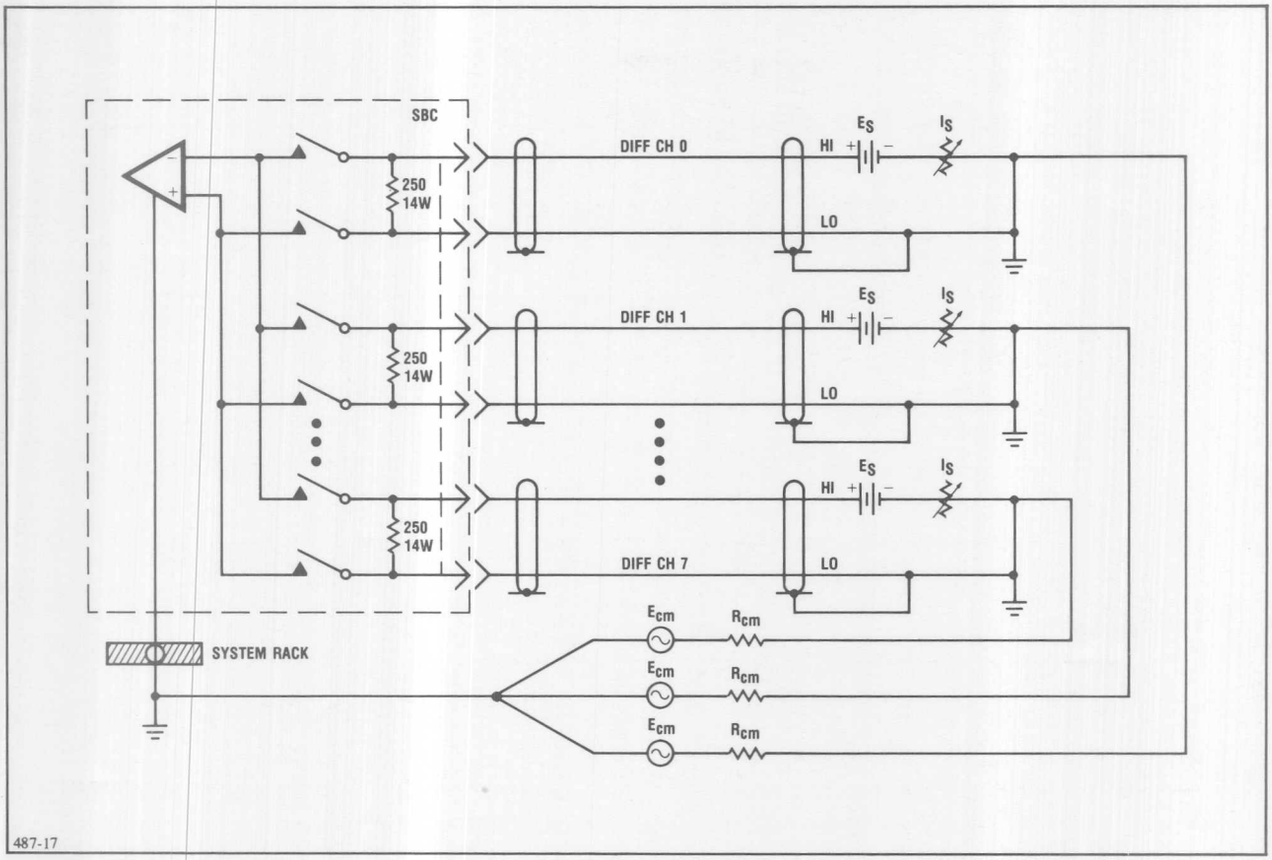


Figure 2-8. Current Source Input Cabling

2-19. BOARD INSTALLATION

CAUTION

Always turn off the computer before installing or removing the SBC 711 board and before installing or removing device interface cables. Failure to take this precaution can result in damage to the board.

In an SBC 80 Single Board Computer based system, install the SBC 711 in any slot that has not been wired for a dedicated function. In an Intellec Microcomputer Development System, install the SBC 711 in any slot except slots 1 and 2. Ensure that auxiliary connector P2 (if used) mates with the user-installed mating connector. Attach the analog input cable assembly to connectors J2 (and to connector J3 if optional multiplexers have been installed).

IMPORTANT

If the SBC 711 is installed in an Intellec System, the Advanced Write option of the CPU board must be modified by removing jumper C-D and installing jumper D-E. This will make the Intellec System CPU Memory Write timing compatible with the Multibus timing requirements.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter illustrates and describes the command, status, and data formats for programming the ADC channels. Also included are several program examples for analog input operation.

3-2. MEMORY BASE ADDRESS

The system computer communicates with the SBC 711 through a sequence of Read and Write commands. The memory addresses used for these commands are relative to a 16-bit memory base address (M) that must lie on a 16-byte boundary. The memory base address (M) is configured at the factory to F700; however, the base address may be reconfigured as described in paragraph 2-9.

3-3. MEMORY ADDRESS ASSIGNMENTS

Table 3-1 lists the individual commands associated with the SBC 711 Analog-to-digital converter (ADC). These commands are addressed as specific memory locations relative to the memory base address (M). If, for example, the memory base address is F700, the address M+5 implies the specific memory address F705.

3-4. READ/WRITE FORMATS

3-5. MULTIPLEXER ADDRESS AND GAIN

The multiplexer (MUX) address and gain format is shown in figure 3-1. Bits 0-4 select the desired channel (starting channel for a sequential scan), bit 5 is ignored, and bits 6-7 select the desired Programmable Gain Amplifier (PGA) input voltage gain. Table 3-2 lists the recommended programmable gain versus the ADC full-scale input voltage range. (The ADC input voltage range and polarization are jumper-selectable as described in paragraph 2-11.)

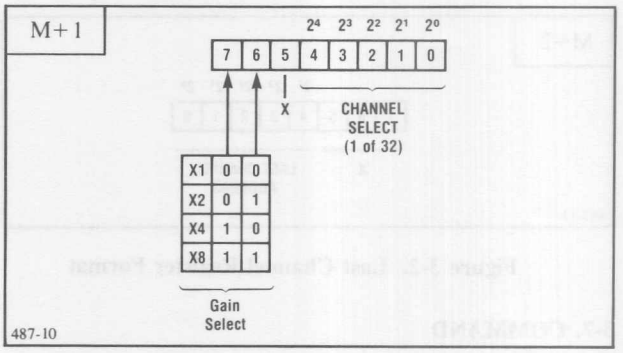


Figure 3-1. MUX Address and Gain Format

Table 3-1. Memory Address Assignments

MEMORY ADDRESS	COMMAND	FUNCTION
M+0	Write	Load Command Register
M+0	Read	Read Status Register
M+1	Write	Load MUX Address Register and Gain Register
M+1	Read	Read MUX Address Register and Gain Register
M+2	Write	Load Last Channel Register
M+3	Write	Clear Interrupts
M+4	Read	Read Lower Byte of ADC Value
M+5	Read	Read Upper Byte of ADC Value

Table 3-2. Programmable Gain Vs ADC Full-Scale Range

ADC FULL-SCALE RANGE				GAIN
+5V	+10V	±5V	±10V	
+5V	+10V	±5V	±10V	X1
+2.5V	+5V	±2.5	±5V	X2
+1.25V	+2.5V	±1.25	±2.5	X4
+0.625V	+1.25V	±0.625V	±1.25	X8

The MUX address and gain are established by performing a Write to M+1; the MUX address and gain may be verified by performing a Read of M+1.

3-6. LAST CHANNEL

For sequential channel scan operation, the starting address is written into the MUX Address Register (M+1) and the ending address is written into the Last Channel Register (M+2). The format of last sequential address is illustrated in figure 3-2.

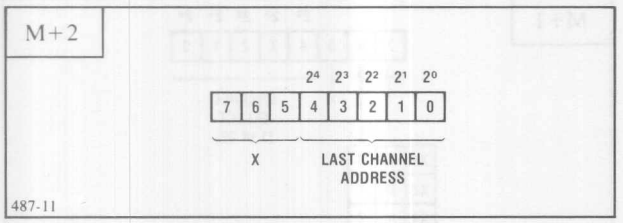


Figure 3-2. Last Channel Register Format

3-7. COMMAND

The Command Register, which is associated entirely (either directly or indirectly) with the A/D conversion process, is loaded by a Write Command to M+0. Bit 0 *must* be set before the A/D conversion can occur, bit 1 is set *only* when a sequential scan is desired, and bit 2 is set when an external trigger is used to start the conversion process. Bit 3 is used to clear the "busy status" bit. Bits 4 and 5, when set, enable the End-of-Scan (EOS) and End-of-Conversion (EOC) interrupts, respectively. The Command Register format is shown in figure 3-3; notice that bits 6 and 7 are not used.

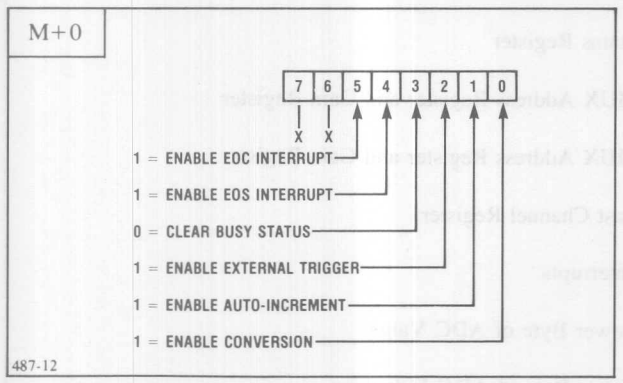


Figure 3-3. Command Register Format

3-8. STATUS

The contents of the Status Register, which contains the status of the ADC and the functions associated with the A/D conversion process, are accessed by a Read Command to M+0. As shown in figure 3-4, bits 0 through 5 essentially verify the last command word written into M+0. (See figure 3-3.) Bit 3 (Board Busy), however, has a special function. The first time a Read Command to M+0 is performed after the Busy Status bit is cleared by a Write to M+0, the Board Busy bit will be read as a "0". Each time thereafter that the Status Register is read, the Board Busy bit will be returned true. This function is useful for multiprocessor systems in which two or more processors are sharing the SBC 711 and require a "semaphore." Note that the Board Busy bit can be cleared only by Write Command to M+0 with bit 3 clear.

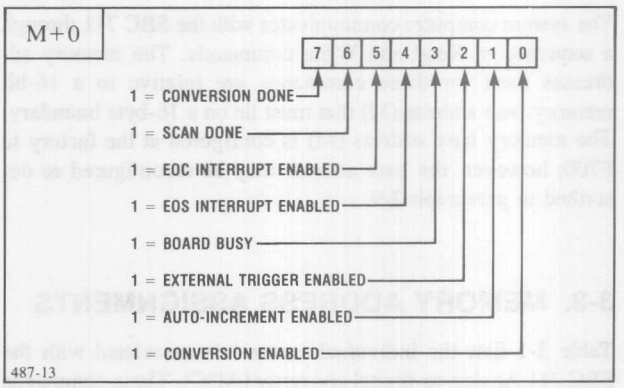


Figure 3-4. Status Register Format

Bits 6 and 7 are for use primarily in non-interrupt driven programs to determine when valid ADC data is ready to be read (Conversion Done) and when the last channel has been converted (Scan Done).

3-9. CLEAR INTERRUPT BIT

Interrupt bits may be individually or collectively cleared by a Write Command to M+3 using the format shown in figure 3-5.

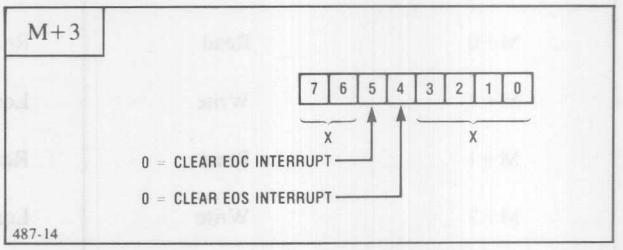


Figure 3-5. Clear Interrupt Bit Format

3-10. ADC DATA

After the A/D conversion is complete, the data word is obtained by a Read Command to M+4 and a Read Command to M+5.

As shown in figure 3-6, M+4 contains the ADC bits 0 through 3 and M+5 contains ADC bits 4 through 11.

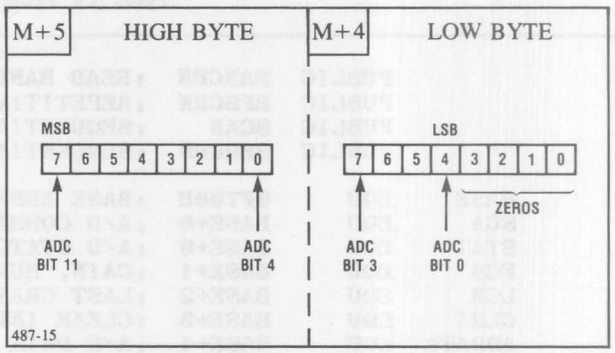


Figure 3-6. ADC Data Format

3-11. PROGRAMMING EXAMPLES

Table 3-3 provides examples of an assembly language program that includes both interrupt driven and non-interrupt driven subroutines for controlling the A/D conversion process. An assembly language program used only for calibration of the ADC is presented in Appendix A. The calibration program is provided to support the calibration procedures contained in Chapter 5.

Table 3-3. Programming Examples

```
        PUBLIC  RANCHN  ;READ RANDOM CHANNEL.
        PUBLIC  RPSCHN  ;REPETITIVE SINGLE CHANNEL, INTERRUPT.
        PUBLIC  SCAN    ;SEQUENTIAL CHANNEL, NON-INTERRUPT.
        PUBLIC  SEQCHN  ;SEQUENTIAL CHANNEL, INTERRUPT.

BASE    EQU     0F700H  ;BASE ADDRESS OF INTERFACE.
SCA     EQU     BASE+0  ;A/D COMMAND REGISTER.
STAT    EQU     BASE+0  ;A/D STATUS REGISTER.
FCR     EQU     BASE+1  ;GAIN, MUX ADDRESS REGISTER.
LCR     EQU     BASE+2  ;LAST CHANNEL REGISTER(WRITE ONLY).
CLRI    EQU     BASE+3  ;CLEAR INTERRUPTS.
ADDATA  EQU     BASE+4  ;A/D DATA REGISTER.
GO      EQU     1       ;CONVERSION-ENABLE IN COMMAND REGISTER.
AIE     EQU     2       ;AUTO-INCREMENT ENABLE BIT.
ETE     EQU     4       ;EXTERNAL-TRIGGER ENABLE BIT.
BUSY    EQU     8       ;MULTI-PROCESSOR BUSY BIT.
EOSIE   EQU     10H     ;EOS INTERRUPT ENABLE.
EOCIE   EQU     20H     ;EOC INTERRUPT ENABLE.
EOS     EQU     40H     ;EOS STATUS.
EOC     EQU     80H     ;EOC STATUS.
CHAN0   EQU     0       ;CHANNEL 0.
X1      EQU     0       ;GAIN = 1.
X2      EQU     040H    ;GAIN = 2.
X4      EQU     080H    ;GAIN = 4.
X8      EQU     0C0H    ;GAIN = 8.

;THE FOLLOWING IS A LIST OF ALL PUBLIC VARIABLES USED IN THIS MODULE.
        DSEG
GAIN:   DS      1       ;(0,1,2, OR 3)
FSTCHN: DS      1       ;(0-31)
LSTCHN: DS      1       ;(0-31)
DATPTR: DS      2       ;POINTER TO DATA FIELD.
ISR6V:  DS      2       ;POINTER TO INTERRUPT 6 SERVICE ROUTINE.

;*****************************************************************
;THE FOLLOWING IS A LIST OF ALL THE INTERRUPT PROCEDURES USED.
;*****************************************************************

;*****************************************************************
;ISR6 IS USED TO SERVICE EOC INTERRUPTS. THE USER MUST STORE THE
;ADDRESS OF THE ACTUAL ISR IN 'ISR6V'.

        ORG     30H     ;INTERRUPT 6 (EOC ISR)
ISR6:   PUSH    H       ;SAVE HL.
        LHLD    ISR6V   ;LOAD POINTER TO SUBROUTINE.
        XTHL            ;RESTORE HL.
        RET             ;JMP TO SERVICE ROUTINE.

;*****************************************************************
;ISR7 IS USED TO SERVICE EOS INTERRUPTS FOR SEQUENTIAL CHANNEL MODE.

        ORG     38H     ;INTERRUPT 7 (EOS ISR)
ISR7:
EOSISR: PUSH    H       ;SAVE HL.
        LXI     H,ISR6B ;POINT TO ALTERNATE ISR.

        SHLD    ISR6V   ;CHANGE INTERRUPT 6 SERVICE ROUTINE.
        POP     H       ;RESTORE HL.

        PUSH    PSW     ;SAVE FLAGS.
        MVI     A,NOT EOSIE     ;CLEAR EOS INTERRUPT.
        STA     CLRI
        POP     PSW     ;RESTORE FLAGS.

        EI              ;RE-ENABLE INTERRUPTS.
        RET             ;EXIT ISR7.
```

Table 3-3. Programming Examples (Continued)

```
;*****************************************************************
;SUBROUTINE ISR6A IS THE EOC INTERRUPT SERVICE ROUTINE THAT IS
;USED WHEN MORE CHANNELS ARE TO BE CONVERTED, SUCH AS IN
;REPETITIVE SINGLE CHANNEL MODE, OR IN SEQUENTIAL CHANNEL MODE.

        CSEG
ISR6A:  PUSH    H           ;SAVE REGISTERS.
        PUSH    D
        PUSH    PSW
        LXI     H,CLRI      ;CLEAR EOC INTERRUPT.
        MVI     M,NOT EOCIE

        CALL    LDDATA      ;LOAD CONVERTOR DATA INTO MEMORY.
        POP     PSW         ;RESTORE REGISTERS.
        POP     D
        POP     H
        EI                  ;RE-ENABLE INTERRUPTS.
        RET                 ;EXIT ISR6A.

;*****************************************************************
;ISR6B IS THE EOC INTERRUPT SERVICE ROUTINE THAT IS USED
;FOR READING THE DATA FROM THE LAST CHANNEL THAT IS TO BE
;CONVERTED IN SEQUENTIAL CHANNEL MODE.

        CSEG
ISR6B:  PUSH    H           ;SAVE REGISTERS.
        PUSH    D
        PUSH    PSW
        LXI     H,SCA       ;CLEAR COMMAND REGISTER BEFORE
        MVI     M,0         ;LOADING A/D DATA INTO MEMORY.
        CALL    LDDATA      ;LOAD CONVERTOR DATA INTO MEMORY.
        POP     PSW         ;RESTORE REGISTERS.
        POP     D
        POP     H
        RET

;*****************************************************************
;'ISR6C' IS THE EOC SERVICE ROUTINE FOR THE REPETITIVE-SINGLE-
;CHANNEL MODE PROCEDURE, 'RPSCHN'.

        CSEG
ISR6C:  PUSH    H           ;SAVE REGISTERS.
        PUSH    D
        LHLD    ADDATA      ;LOAD CONVERTOR DATA.
        XCHG

        LHLD    DATPTR      ;LOAD POINTER TO DATA FIELD.
        MOV     M,E         ;LOAD CONVERTOR DATA INTO MEMORY.
        INX     H
        MOV     M,D
        POP     D           ;RESTORE REGISTERS.
        POP     H

        PUSH    PSW         ;SAVE FLAGS.
        MVI     A,NOT EOCIE;CLEAR EOC INTERRUPT.
        STA     CLRI
        POP     PSW         ;RESTORE FLAGS.
        EI                  ;ENABLE INTERRUPTS.
        RET                 ;EXIT ISR6C

;*****************************************************************
;SUBROUTINE RANCHN USES THE GLOBAL VARIABLES 'FSTCHN' AND 'GAIN'
;TO DEFINE THE CHANNEL AND GAIN TO BE USED IN THE CONVERSION
;OF THE ANALOG INPUT. THE RESULT IS STORED AT THE LOCATION
;POINTED BY 'DATPTR'.
```

Table 3-3. Programming Examples (Continued)

```
        CSEG
RANCHN: LXI     H,FCR   ;POINT HL TO FIRST CHANNEL REGISTER.
        LDA     GAIN    ;LOAD GAIN.
        MOV     C,A
        LDA     FSTCHN  ;LOAD CHANNEL.
        ORA     C       ;ADD GAIN BITS.
        MOV     M,A     ;LOAD FIRST CHANNEL REGISTER.

        DCX     H       ;POINT TO COMMAND/STATUS REGISTER.
        MVI     M,GO    ;START A/D CONVERSION.

RAN1:   MOV     A,M     ;READ STATUS.
        RLC             ;CHECK EOC STATUS.
        JNC     RAN1    ;JMP IF CONVERSION NOT DONE.

        MVI     M,0     ;RESET CONVERSION-ENABLE IN COMMAND REGISTER.
        CALL    LDDATA  ;LOAD CONVERSION DATA INTO DATPTR.

        RET             ;EXIT RANCHN.

;*****************************************************************
;SUBROUTINE 'SCAN' USES THE GLOBAL VARIABLES 'FSTCHN', 'LSTCHN',
;AND 'GAIN' TO DEFINE THE FIRST CHANNEL, LAST CHANNEL AND GAIN
;TO BE USED FOR THE SEQUENTIAL CHANNEL MODE. THE DATA IS STORED
;IN CONSECUTIVE MEMORY LOCATIONS, STARTING WITH THE LOCATION
;POINTED BY 'DATPTR'.

        CSEG
SCAN:   LXI     H,LCR   ;POINT HL TO LAST CHANNEL REGISTER.
        LDA     LSTCHN  ;LOAD LAST CHANNEL.
        MOV     M,A

        DCX     H       ;POINT HL TO FIRST CHANNEL REGISTER.
        LDA     GAIN
        MOV     C,A

        LDA     FSTCHN  ;LOAD FIRST CHANNEL.
        ORA     C       ;ADD GAIN BITS.
        MOV     M,A     ;LOAD FIRST CHANNEL REGISTER.

        DCX     H       ;POINT TO COMMAND/STATUS REGISTER.
        MVI     M,CO OR AIE OR ETE;START SCAN MODE W/EXTERNAL TRIGGER.

SCAN1:  MOV     A,M     ;READ STATUS.
        RAL             ;CHECK EOS.
        RAL
        JC      SCAN2   ;JMP IF MAR=LCR.
        RAR             ;CHECK EOC.
        JNC     SCAN1   ;JMP IF CONVERSION NOT DONE.
        CALL    LDDATA  ;LOAD DATA FROM CONVERTOR.
        LXI     H,STAT  ;POINT HL TO STATUS REGISTER.
        JMP     SCAN1   ;START NEXT CONVERSION.

SCAN2:  MOV     A,M     ;CHECK FOR LAST CHANNEL EOC.
        RLC
        JNC     SCAN2   ;JMP IF LAST CHANNEL NOT DONE.

        MVI     M,0     ;TURN OFF CONVERTOR.
        CALL    LDDATA  ;LOAD DATA FROM CONVERTOR.
        RET             ;EXIT SCAN.

;*****************************************************************
;SUBROUTINE 'LDDATA' TAKES THE A/D CONVERTOR DATA AND
;LOADS IT INTO THE MEMORY LOCATIONS POINTED BY 'DATPTR'.
```

Table 3-3. Programming Examples (Continued)

```
          CSEG
LDDATA:   LHLD    ADDATA   ;LOAD CONVERTOR DATA INTO HL.
          XCHG               ;PUT DATA INTO DE.
          LHLD    DATPTR   ;LOAD POINTER TO DATA FIELD.
          MOV     M,E      ;STORE DATA IN MEMORY.
          INX     H
          MOV     M,D
          INX     H
          SHLD    DATPTR   ;SAVE NEW POINTER.
          RET              ;EXIT LADATA.

;*************************************************************
;SUBROUTINE 'SEQCHN' IS AN EXAMPLE OF AN INTERRUPT-DRIVEN
;PROCEDURE WHICH WILL LOAD DATA FROM THE A/D CONVERTOR USING
;THE SEQUENTIAL-CHANNEL MODE. JUMPERS (95,96) AND (38,40)
;MUST BE CONNECTED TO ALLOW THE CRYSTAL CLOCK TO GENERATE
;TRIGGER COMMANDS. JUMPER (79,81) MUST BE CONNECTED TO ALLOW
;EOC TO GENERATE AN INTERRUPT ON INT6/, AND JUMPER (78,80)
;MUST BE CONNECTED TO ALLOW EOS TO GENERATE AN INTERRUPT
;ON INT7/.

          CSEG
SEQCHN:   LXI     H,ISR6A  ;INITIALIZE ISR6 VECTOR ADDRESS.
          SHLD    ISR6V

          LXI     H,LCR    ;POINT TO LAST CHANNEL REGISTER
          LDA     LSTCHN   ;LOAD LAST CHANNEL.
          MOV     M,A

          DCX     H        ;POINT TO MUX ADDRESS REGISTER.
          LDA     GAIN     ;LOAD GAIN BITS.
          MOV     C,A
          LDA     FSTCHN   ;LOAD FIRST CHANNEL.
          ORA     C        ;ADD GAIN BITS.
          MOV     M,A      ;LOAD MUX ADDRESS REGISTER.

          DCX     H        ;POINT TO COMMAND REGISTER.
          MVI     M,GO OR AIE OR ETE OR EOCIE OR EOSIE;LOAD COMMAND.
          EI               ;ENABLE INTERRUPTS.
          RET              ;WAIT FOR EOC.

;*************************************************************
;SUBROUTINE 'RPSCHN' IS AN EXAMPLE OF AN INTERRUPT-DRIVEN
;PROCEDURE WHICH PERFORMS REPETITIVE-SINGLE-CHANNEL CONVERSIONS.
;JUMPERS (38,40) AND (95,96) MUST BE CONNECTED TO ALLOW THE CLOCK
;TO TRIGGER A/D CONVERSIONS, AND JUMPER (79,81) MUST BE CONNECTED
;TO ALLOW EOC TO GENERATE INTERRUPTS ON INT6/.

          CSEG
RPSCHN:   LXI     H,ISR6C  ;INITIALIZE ISR6 VECTOR ADDRESS.
          SHLD    ISR6V

          LXI     H,FCR    ;POINT TO MUX ADDRESS REGISTER.
          LDA     GAIN     ;LOAD GAIN BITS.
          MOV     C,A
          LDA     FSTCHN   ;LOAD CHANNEL # .
          ORA     C        ;ADD GAIN BITS.
          MOV     M,A      ;LOAD MUX ADDRESS REGISTER.

          DCX     H        ;POINT TO COMMAND REGISTER.
          MVI     M,GO OR ETE OR EOCIE;START FIRST CONVERSION.
          EI               ;ENABLE INTERRUPTS.
          RET

          END
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description and a circuit analysis of the SBC 711 Analog Input Board.

4-2. FUNCTIONAL DESCRIPTION

The SBC 711 consists of the following seven functional blocks (refer to figure 4-1):

a. Analog Input Multiplexer

b. Programmable Gain Amplifier (PGA)

c. Sample-and-Hold (S/H) Amplifier

d. Analog-to-Digital Converter (ADC)

e. DC/DC Converter

f. Control and Bus Interface Logic

4-3. ANALOG INPUT MULTIPLEXER

The Analog Input Multiplexer is located in the ADC module and may be configured by the user to provide either 8 differential of 16 single-ended analog input channels. Sockets are provided so that the multiplex capability can optionally be expanded to accommodate an additional 8 differential or 16 single-ended channels by installing two 16-pin dual in-line package (DIP) multiplexers (Harris H1818A's or equivalent). All input channels are protected to ±28V by clamping diodes and fusible current-limit resistors; this insures the board against potentially destructive overloads under fault conditions.

The differential input channels have provisions for the installation of discrete 250-ohm ±1.0% 1/4W resistors in order to accept 4- to 20-mA current loop inputs. The temperature coefficient of these resistors must be <0.01%/°C.

There are three programmable modes of operation for the acquisition and conversion of analog inputs: random channel input, repetitive single channel input, and sequential channel scan input. The multiplexer address is selected by writing to the Multiplexer Address Register, which is physically located inside the ADC module. (The most significant bit of the multiplexer address is stored in a separate register).

The selected analog output signal is applied to the input of the Programmable Gain Amplifier.

4-4. PROGRAMMABLE GAIN AMPLIFIER

The selected analog channel from the multiplexer is applied to the input of the Programmable Gain Amplifier (PGA). The output of the PGA, which provides program-controlled gains of X1, X2, X4, and X8, is applied to a Sample-and-Hold (S/H) amplifier contained in the ADC module.

4-5. SAMPLE-AND-HOLD AMPLIFIER

The S/H Amplifier, which is physically located inside the ADC module, tracks the PGA output voltage until a trigger signal is received. This trigger signal can be input from the on-board pacer clock or from an external source, or can be program initiated. When the trigger signal is received, the S/H Amplifier switches from the sample (tracking) mode to the hold mode and the A/D conversion process starts.

4-6. ANALOG-TO-DIGITAL CONVERTER

The ADC uses the successive approximation technique, implementing a high-speed, closed-loop servo to arrive at a digital output representing the value of the input signal. The 12-bit A/D conversion cycle is completed in approximately 35.7 microseconds. The ADC module outputs an End-of-Conversion signal to indicate when the conversion is complete. After the most-significant data byte has been read, the ADC module is ready for a new conversion process.

4-7. DC-DC CONVERTER

The DC-DC Converter converts the +5V logic supply input to regulated and filtered ±15V required by the analog circuits. For special applications, the SBC 711 may be configured to operate in a low-power mode. The low-power mode is useful when the SBC 711 is being used in systems with the +5V logic supply operating at near full capacity. The DC-DC Converter module may be removed and an external ±15V regulated power supply may be used to power the analog circuits.

4-8. CONTROL AND BUS INTERFACE

The Bus Interface logic consists of those circuit elements most directly associated with the Multibus. These circuit elements include memory base address detection logic, memory Read and Write decoders, transfer acknowledge generation logic, input and output data buffers, interrupt drivers, and ROM and PROM inhibit drivers.

The control logic receives outputs from the Read and Write decoders and input data buffers to provide control signals for the various registers and timing logic.

4-9. CIRCUIT ANALYSIS

The schematic diagram for the SBC 711 is given in figure 5-2. The schematic diagram consists of two sheets, each of which includes grid coordinates. In the following paragraphs, a reference such as 2ZF5 will locate the subject circuit on sheet 2 in Zone F5.

Both active-high and active-low signals are used. A signal mnemonic that ends with a slash (e.g., MWTC/) or includes an overscore (e.g., $\overline{\text{STR}}$) denotes that the signal is active-low. Conversely, a signal without a slash or an overscore denotes that the signal is active-high.

No detailed discussion is included for the ADC and DC-DC modules. These modules are replaceable as a unit part.

4-10. INITIALIZATION

System Initialize signal INIT/ is driven low on the Multibus when power is initially applied to the system or whenever the computer "reset" function is performed. The INIT/ signal is buffered by A35-11 (1ZH8) to clear Command Register A36.

4-11. BASE ADDRESS DECODING

The system processor communicates with the SBC 711 by issuing Memory Read and Memory Write Commands. As described in paragraph 2-9, the memory addresses used for these commands are relative to a 16-bit address that must lie on a 16-byte boundary; this memory base address is assigned by the user by means of jumper wires installed in a 16-pin DIP header. The configured DIP header is then installed in IC socket M4 (1ZF3) to control an array of 12 open-collector exclusive-OR gates contained in A22, A32, and A33.

Address bits ADR4/ through ADRF/ are decoded by the exclusive-OR gates. When the memory base address is true (i.e., matches the jumper configuration of M4), the output of each exclusive-OR gate remains high to generate the Base Address Enable (BAE) signal. The BAE signal is inverted to produce the BAE/, INH1/, and INH2/ signals. The BAE/ signal is applied as an enable input to A13-10 and A13-13 (1E16) to allow these NOR-gates to respond respectively to Memory Read and Memory Write Commands. The BAE/ signal also holds one input low to each of NOR-gate input data buffers A25 and A26 (1ZH16).

The SBC 711 fully supports the Multibus memory inhibit capability. This permits the SBC 711 to overlay any system RAM or ROM, with only a slight loss in system speed. The INH1/ (Inhibit RAM) and INH2/ (Inhibit ROM) signals prevent those memory addresses from responding to the same addresses as the SBC 711.

The SBC 711 generates INH1/ and INH2/ whenever it is addressed within the range determined by the jumper wires installed in M4. These signals must be of sufficient duration to prevent the inhibited board from responding to the same addresses. This time duration, which is solely a function of the inhibited board, must be determined from the specifications of that board. Since INH1/ and INH2/ are generated from the address on the Multibus, the only way the SBC 711 can control the pulse width of INH1/ and INH2/ is by delaying the XACK/ signal in response to a Memory Read (MRDC/) or Memory Write (MWTC/) command. Refer to table 2-10 for the connections required to generate the appropriate signal pulse widths for INH1/ and INH2/. Note that the SBC 711 is set at the factory for a minimum XACK/ delay, which assumes that it is to be used in the non-overlapped mode.

4-12. COMMAND DECODING

A Transfer Acknowledge (XACK/) signal is returned on the Multibus by the SBC 711 to specify that it has completed the specified Memory Read or Memory Write operation. When either an MRDC/ or MWTC/ is accepted (i.e., BAE/ is true), the output of A13-4 (1ZB15) loads counter A31 and provides an enable input to gate A15-11. The value loaded into counter A31 is determined by the jumper wires installed as described in paragraph 2-14. The counter is clocked by CCLK/ and, when the full count of A31 is reached, the next high-to-low transition of CCLK/ causes the CY output of A31 to go low and generate XACK/. The CY output is also fed back to the input of A30-11 to inhibit further clock inputs to the counter until the counter is reloaded when MRDC/ or MWTC/ is inactive.

4-13. WRITE COMMANDS. All Memory Write Commands relative to the base address are decoded by A15 (1ZD15). The Memory Write Command (MRDC/) is inverted by A13-13 and applied to the inputs of A14-3 and A14-11. Address bit ADR3/ controls the enable inputs to decoder A15: if ADR3/ is high, the output of A14-3 pulls the 1G input low and enables the 1Y0 through 1Y3 functions. (The 2Y0 through 2Y3 functions are not used.) With its 1G input low, A15 decodes address bits ADR0/ and ADR1/ and activates the appropriate signal listed in table 4-1.

4-14. READ COMMANDS. All Read Commands (except Read Multiplexer Address and Gain) relative to the base address are decoded by A16 (1ZF15). The Memory Read Command (MRDC/) is inverted by A13-10 and applied to the input of A14-8. If either ADR1/ or ADR3/ (or both) is low, the output of A13-10 goes low and enables A16 at its 2G input. Address bits ADR0/ and ADR2/ are then decoded as listed in table 4-2. The

Table 4-1. Write Command Decoder A15 Output Signals

MULTIBUS ADDRESS BITS*				SIGNAL MNEMONIC	SIGNAL DEFINITION
ADR3/	ADR2/	ADR1/	ADR0/		
1	1	1	1	WCR/	Write to Command Register
1	1	1	0	WMAR/	Write to Multiplexer Address Register (includes channel gain)
1	1	0	1	WLCR/	Write to Last Channel Register
1	1	0	0	WINT/	Write (Clear) Interrupt

*Address bits are complemented by the system processor before placing them on Multibus. Address bit ADR2/ is not relevant to decoder A15. All commands require MWTC/ to be active.

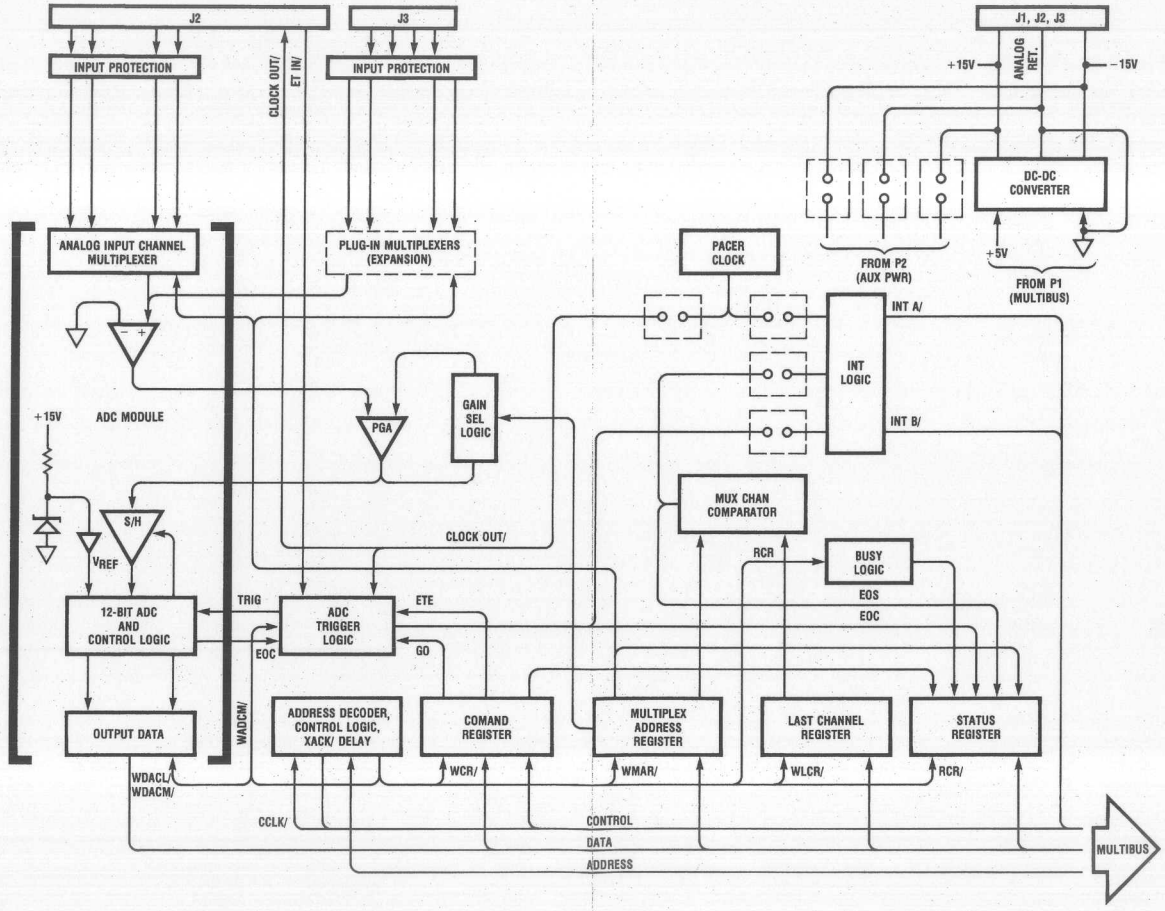


Figure 4-1. SBC 711 Block Diagram

Table 4-2. Read Command Decoder A16 Output Signals

MULTIBUS ADDRESS BITS*				SIGNAL MNEMONIC	SIGNAL DEFINITION
ADR3/	ADR2/	ADR1/	ADR0/		
1	1	1	1	RCR/	Read Status (Command) Register
1	0	1	1	RADCL/	Read ADC Least-Significant (Low) Byte
1	0	1	0	RADCM/	Read ADC Most-Significant (High) Byte

*Address bits are complemented by the system processor before placing them on Multibus. All commands require MRDC/ to be active.

Multiplexer Address and Gain is read by performing a Read Command to M+1 as described in paragraph 4-18.

4-15. DATA BUFFERS

When a Write Command is received, data bits DAT0/ through DAT7/ are gated onto the board and inverted by to A25 and A26 to produce Input Data Transfer signals IDT0 through IDT7. When a Read Command is received, Output Data Transfer signals ODT0/ through ODT7/ are driven through buffers A34 and A35 onto Multibus data lines DAT0/ through DAT7/. (Refer to 1ZH16.)

4-16. REGISTERS

4-17. COMMAND REGISTER. The Command Register (CR) is loaded by a Write Command to M+0, which activates the WCR/ output of decoder A15. The leading edge of the WCR/ signal, which is driven through inverter A17-8, clocks the command word present on IDT0 through IDT5 into Command Register A36 (1ZH8). Output signals from the Command Register are as follows:

a. GO (Enable Conversion)—This signal sets TADC flip-flop A19-11 when clocked by the trailing edge of the WCR/ signal or by the trailing edge of the RADCM/ signal. The TADC flip-flop and associated gates allow the A/D conversion to be controlled by the on-board Pacer Clock, an external trigger, or by the GO bit itself.

b. AIE (Auto-Increment Enable)—This signal generates (via A28-11) the $\overline{\text{STR}}$ signal, which is applied to the multiplexer address counter in the ADC module.

c. ETE (External Trigger Enable)—This signal is used in the TADC circuit to allow the ADC to be triggered by the internal Pacer Clock (CLOCK OUT/) or by an external trigger (ET IN/).

d. EOSIE (End-of-Scan Interrupt Enable)—This signal removes the inhibit (reset) input at pin 1 of INTA flip-flop A12-3. This allows A12-3 to be clocked by an EOS (End-of-Scan) signal or an RTC (Real Time Clock) signal to generate a system interrupt.

e. EOCIE (End-of-Conversion Interrupt Enable)—This signal removes the inhibit (reset) input at A12-13 of the INT B flip-flop. This allows A12-11 to be clocked by an EOC (End-of-Conversion) signal to generate a system interrupt.

The Clear Busy status bit (bit 3) of the command word is not latched into Command Register A36. With the IDT3 bit false, the WCR/ signal inhibits A28-6, which clears BUSY flip-flop A19-3 (1ZC8).

4-18. MULTIPLEXER ADDRESS REGISTER. The Multiplexer Address Register (MAR) is contained in ADC module M3 (2ZD6). The MAR is loaded by a Write Command to M+1, which activates the WMAR/ output of decoder A15. When WMAR/ goes low, the contents of IDT0 through IDT3 are loaded into M3. The WMAR/ signal also clocks the LD input of register A18 which latches in IDT4, IDT6, and IDT7. The outputs of A18 are used as follows:

a. G0 and G1, developed from IDT6 and IDT7, control the gain of Programmable Gain Amplifier A4 (2Z19).

b. MAR CH16, developed from IDT4, is decoded by A11 (2Z17) to extend the addressing capability to 32 channels (assuming multiplexers A2 and A5 are installed).

The contents of the MAR is read by a Read Command to M+1. Bit ADR0/ is inverted by A23-4 to hold pin 1 high to multiplexers A37 and A38 (1ZE13); bit ADR2/ is inverted by A23-12 to hold pin 15 low at A37 and A38. With pins 1 and 15 thus enabled, the "B" inputs supplied by the MAR are selected, complemented, and driven onto the Multibus.

4-19. LAST CHANNEL REGISTER. The Last Channel Register (LCR) is loaded by a Write Command to M+2, which activates the WLCR/ output of decoder A15. When WLCR/ goes low, the contents of IDT0 through IDT4 are loaded into register A27 (1ZI11). The outputs of A27 are applied to comparator A29.

4-20. STATUS REGISTER. Command Register A36 also serves as part of the Status Register. The status of the SBC 711 is ascertained by a Read Command to M+0. Bit ADR0/ is inverted by A23-4 to hold pin 1 low at multiplexers A37 and A38; bit ADR2/ is inverted by A23-12 to hold pin 15 low at A37-A38. With both pins 1 and 15 of A37-A38 low, the "A" inputs supplied by the Command Register are selected, complemented, and driven onto the Multibus.

The Read Command to M+0 is decoded by A16, which activates the RCR/ output. The trailing edge of the RCR/ signal clocks flip-flop A19-3 (1ZC8) and clears the BUSY status signal. The first time a Read Command to M+0 is performed after the BUSY status signal is cleared by a Write Command to

M+0, the BUSY status will be read as "0". Each time thereafter that the Status Register is read, the BUSY status will be returned true. This function is useful for multiprocessor systems in which two or more processors are sharing the SBC 711 and require a "semaphore". Note that the BUSY status can be cleared only by Write Command to M+0 with bit 3 clear.

4-21. ANALOG INPUT OPERATION

The following paragraphs describe random channel, repetitive single channel, and sequential channel scan operation for A/D data acquisition; all channel references assume that the SBC 711 is configured for single-ended multiplexing.

4-22. RANDOM CHANNEL. Random channel operation begins by performing a Write Command to M+1. When the BAE/ signal goes true, A15 decodes ADR0/ through ADR3/ and drives its WMAR/ output signal low. The leading edge of the WMAR/ signal (1) clocks register A18 to latch in the gain select bits (IDT6 and IDT7) and the most-significant channel select-bit (IDT4) and (2) drives the ADC module (M3) Load Enable input low. The WMAR/ signal is also driven through A21-11 and inverter A17-6 to develop strobe signal $\overline{\text{STR}}$. On the trailing edge of $\overline{\text{STR}}$, the counter in the ADC module latches in the multiplexer address bits specified by IDT0 through IDT3. The counter, which is not incremented in random channel operation, transfers the address internally to the ADC module multiplexer and externally to the user-installed multiplexers (A2 and A5) via the MAR CH1 through MAR CH8 outputs.

Register A18 outputs MAR CH16 (developed from IDT3) to one input of decoder A11; the second input to A11 is MAR CH8 from the ADC module. The MAR CH16 and MAR CH8 inputs to A11 select one of four multiplexer blocks of eight channels each. For example, if MAR CH16 is high and MAR CH8 is low, the 2Y2 output of A11 is driven low and enables multiplexer A2 (channels 16-23); if MAR CH16 and MAR CH8 are both low, the 2Y0 output of A11 is driven low and (via inverter A10-4) enables the HI EN input (channels 0-7) of the ADC module.

If the multiplexer channels have been expanded by the installation of multiplexer A2 (channels 16-23) and A5 (channels 24-31), the specific address of the enabled multiplexer is determined by the MAR CH1 through MAR CH8 outputs of the ADC module.

The input of the selected multiplexer channel is applied to a unity gain differential amplifier in the ADC module. The signal is then routed out of the ADC module to Programmable Gain Amplifier A4, the gain of which is controlled by the G0 and G1 inputs to multiplexer A11. Assuming a gain of X8 is programmed, G0 and G1 will both be high and drive the 1Y3 output of A11 low. This causes a FET switch closure to occur inside of A6 and connect the junction of R46 and R48 in a feedback loop to the input of the PGA. The amplified output of the PGA is applied to the input of S/H amplifier in the ADC module.

The Write Command to M+1 has now (1) selected the proper multiplexer input channel and (2) amplified the input to the desired level and applied it to the S/H amplifier for tracking. Next, a Write Command to M+0 is given to enable the A/D conversion and specify the parameters for the conversion process. (Refer to paragraph 3-7.) With BAE/ true, A15 decodes ADR0/ through ADR3/ and drives its WCR/ output low to clock Command Register A36. The GO bit out of A36 is applied to the D-input of the TADC flip-flop (A19-12); the ETE (External Trigger Enable) bit is applied to one input of A21-8. When the WCR/ goes false, the TADC flip-flop sets and allows the ADC to be triggered from Pacer Clock A7 or from an External Trigger (assuming the ETE bit is true). If the ETE bit was clear when the Write Command to M+0 occurred, the $\overline{\text{Q}}$ output of A19 goes low on the trailing edge of the WCR/ signal and inhibits A21-6. This causes the TRIG signal to go high and enable A21-3 to trigger the A/D conversion process.

If the ETE bit was set when the Write Command to M+0 occurred, the Q output of A19-9 goes high on the trailing edge of the WCR/ signal and holds one input high to A30-6. The second input in A30-6 is from A9-6, whose inputs are controlled by the CLOCK OUT/ signal from Pacer Clock A7 and the ET IN/ signal from an external trigger source. (Refer to paragraph 2-12 for a description of the internal and external trigger clocks.) When either the CLOCK OUT/ or ET IN/ signal is driven low, A30-6 and A21-8 are inhibited and cause the output of A21-6 to go high to generate the TRIG signal.

When the A/D conversion is complete, the ADC module drives its $\overline{\text{EOC}}$ output low to clear TADC flip-flop A19-13. If Command Register bit 5 (EOCIE) is set, flip-flop A12-11 sets when clocked by the $\overline{\text{Q}}$ output of A19-8 and is inverted by A10-12 to generate the INT B/ signal to signify the end of conversion.

The program can either use the INT B/ interrupt signal or read the SBC 711 status to determine when the conversion is complete (signified when EOC bit 7 is true). To determine the status, a Read Command to M+0 is performed as described in paragraph 4-14. When the converted data is valid, the lower and upper bytes of data are transferred onto the Multibus by performing a Read Command to M+4 and M+5, respectively.

When a Read Command to M+4 is performed, the RADCL/ output of decoder A16 goes low and applies Enable signal $\overline{\text{EN 9-12}}$ to pin 17T of the ADC module. The ADC module then drives the lower (least-significant) byte of data onto the Multibus. When a Read Command to M+5 is performed, the RADCM/ output of decoder A16 goes low and applies Enable signals $\overline{\text{EN 1-4}}$ and $\overline{\text{EN 5-8}}$ to pins 15B and 14T, respectively, of the ADC module. The ADC module then drives the upper (most-significant) byte of data onto the Multibus.

The EOC interrupt (if enabled) must be cleared after each random channel conversion. If operation from the present controller is not completed (e.g., another random channel reading or another mode of operation is to follow immediately) the EOC interrupt is cleared by a Write Command to M+3 with bit 5 clear. The WINT/ signal from decoder A15 and IDT5 bit inhibit NOR-gate A20-4 and reset flip-flop A12-13 via A20-1.

If the present controller is finished with the SBC 711, a Write Command to M+0 with and all zeros word disables the interrupts; clears the busy status; and disables the external trigger, auto-increment, and conversion enable functions.

4-23. REPETITIVE SINGLE CHANNEL. Repetitive single channel operation is almost identical to random channel operation discussed in preceding paragraphs. First the multiplexer address and the PGA gain is set up by a Write Command to M+1 and then the command (with the GO bit enabled and the auto-increment bit disabled) is given by a Write Command to M+0. After EOC (End-of-Conversion) is signified (EOC interrupt or EOC status) for the first reading, the user may optionally read the full data word (both lower and upper bytes) or read only the upper byte.

If the full data word is required, the program must read the lower byte first and then read the upper byte. When a Read Command to M+5 (upper byte) is given, the RADCM/ signal goes low and applies Enable signals $\overline{\text{EN 1-4}}$ and $\overline{\text{EN 5-8}}$ to the ADC module. The ADC module then drives the upper byte of data onto the Multibus, and the internal S/H amplifier goes to the sample mode and tracks the signal on the same channel. The trailing edge of the RADCM/ signal clocks flip-flop A19B and arms the TADC circuit.

After the first conversion data is obtained, subsequent conversions are initiated by a Read Command to M+5. As previously mentioned, if the full 12-bit word is desired, the lower byte *must* be read first from M+4 followed by a read of the upper byte from M+5. If only the upper byte is required, a read of M+5 will place the upper byte on the Multibus and automatically perform a new conversion on the same channel when RADCM/ goes high or, if the ETE bit is set in the Command Register, when the CLOCK OUT/ signal or ET IN/ signal is driven low.

4-24. SEQUENTIAL CHANNEL SCAN. The sequential channel scan operation converts the voltage on a specified starting channel to digital data, automatically advances to and converts the next sequential channel when the preceding channel has been read, and repeats this process until the last channel has been converted and read. After each channel input has been converted to digital data, the SBC 711 generates an EOC (End-of-Conversion) signal as previously described. When the last channel has been converted, an EOC signal and an EOS (End-of-Scan) signal are generated. Each of these signals may be used to generate a unique system interrupt, or they may be read as part of the status word. Much of the sequential channel scan operation is identical with that already described for random channel operation in paragaph 4-22. In the following discussion, only those portions that are unique to sequential channel scan operation will be discussed in any detail.

The first step of a sequential channel scan operation is to load the last channel register by performing a Write Command to M+2. Decoder A15 decodes ADR0/ through ADR3/ and drives its WLCR/ output low at the clock input of Last Channel Register A27. Register A27 latches in the last channel address (IDT0 through IDT5) when WLCR/ goes high. The IDT0 through IDT3 (four least-significant address bits) outputs of A27 are applied to one set of inputs of comparator A29 and the IDT4 bit is applied to one input of decoder A16. The next step is to set up the starting channel and PGA gain by performing a Write Command to M+1. Finally, a Write Command to M+0 is given to enable the A/D conversion and specify the parameters for the conversion process. In the sequential channel scan mode, the Enable Auto-Increment bit (bit 1) must be set in order to clock the ADC channel counter, and the GO bit (bit 0) must be set to arm the trigger circuit. The remaining bits of the command word will depend on the program requirements; e.g., bit 2 (ETE) must be set if the CLOCK OUT/ or ET IN/ signal is used to trigger the ADC, and bits 4 and 5 must be set if the program is interrupt driven.

When the A/D conversion is complete, the ADC module drives its $\overline{\text{EOC}}$ output low to clear TADC flip-flop A19-13. If Command Register bit 5 (EOCIE) is set, flip-flop A12-11 sets when clocked by the $\overline{\text{Q}}$ output of A19-8, and is inverted by A10-12 to develop the INT B/ signal to signify the end of conversion.

The program can either use the INT B/ interrupt signal or read the SBC 711 status to determine when the conversion is complete (signified when EOC bit 7 is true). To determine the status, a Read Command to M+0 is performed. When the converted data is valid, the lower and upper bytes of data are transferred onto the Multibus by performing a Read Command to M+4 and M+5, respectively.

When a Read Command to M+4 is performed, the RADCL/ output of decoder A16 goes low and applies Enable signal $\overline{\text{EN 9-12}}$ to pin 17T of the ADC module. The ADC module then drives the lower (least-significant) byte of data onto the Multibus. When a Read Command to M+5 is performed, the RADCM/ output of decoder A16 goes low and applies Enable signals $\overline{\text{EN 1-4}}$ and $\overline{\text{EN 5-8}}$ to pins 15B and 14T, respectively, of the ADC module. The ADC module then drives the upper (most-significant) byte of data onto the Multibus.

The leading edge of the RADCM/ signal generates a $\overline{\text{STR}}$ signal via NAND-gate A21-11 and inverter A17-6 to increment the counter in the ADC module. The multiplexer switches to the new channel and the S/H amplifier begins to track the new signal. The STR signal output of A21-11 is fed to decoder A16 and, whenever STR goes false, the 1Y outputs of decoder A16 are activated. The trailing edge of WADCM/ clocks and sets TADC flip-flop A19-11. The next trigger pulse to the ADC module is automatically generated if the ETE bit is clear; if the ETE bit is set, the trigger pulse is generated when the CLOCK OUT/ or ET IN/ signal is driven low.

This cycle is repeated until the last channel is converted, at which time the ADC module will generate the $\overline{\text{EOC}}$ signals as previously described. However, when the last channel is addressed, the A0 through A3 and A=B IN inputs to comparator A29 will be high. Comparator A29 then drives its A=B OUT status signal high and clocks flip-flop A12-3. If Command Register bit 5 is set, flip-flop A12-3 sets and, via A10-10, generates the INT A/ signal to signify the end of scan.

The EOC interrupt (if enabled) must be cleared after each channel is converted. Both the EOC and EOS interrupt (if enabled) must be cleared after the scan is complete. If operation from the present controller is not completed (e.g., another sequential channel scan or another mode of operation is to follow immediately), the EOC and EOS interrupts are cleared

by a Write Command to M+3 with bits 4 and 5 clear. The WINT/ signal from decoder A15 and IDT4 bit inhibit A20-10 and reset flip-flop A12-1 (EOS) via A20-13. Flip-flop A12B (EOC) is cleared as previously described.

If the present controller is finished with the SBC 711, a Write Command to M+0 with and all zeros word disables the interrupts; clears the busy status; and disables the external trigger, auto-increment, and conversion enable functions.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides calibration procedures, service diagrams, and repair assistance instructions for the SBC 711 Analog Input board.

5-2. CALIBRATION

The calibration procedures presented in following paragraphs should be performed every 90 days or whenever the ADC full-scale range jumpers are reconfigured. The calibration procedures are specifically related to the SBC 711 analog circuits and associated edge connectors; no consideration is given to line losses or correction for transducer offset.

5-3. TEST EQUIPMENT REQUIRED

The following test equipment is required in performing the calibration procedures:

a. Precision Voltage Source; 0 to 15V dc ±0.001%, continuously adjustable; source impedance <1.0 ohm.

b. Digital Multimeter; 0 to 15V dc ±0.001%, 0 to 20 mA ±0.001%.

5-4. PRELIMINARY PROCEDURE

Before beginning the calibration, place SBC 711 on a board extender and verify the dc supply voltages as listed in table 5-1. If any of the supply voltages are out of tolerance, correct the condition before beginning the calibration.

Table 5-1. Power Supply Voltage Checks

SUPPLY	TOLERANCE	VOLTMETER CONNECTIONS*
+15V	±3%	Across C12
−15V	±3%	Across C9
+5V	±5%	Across C44

*Refer to figure 5-1. Capacitor C12 is located in zone C4, capacitor C9 in zone C4, and capacitor C44 in zone B6.

5-5. ADC CALIBRATION PROCEDURE

The calibration procedure for the ADC circuits consists of a three-step sequence which must be performed in the following order: (1) PGA offset adjustment, (2) ADC offset adjustment, and (3) ADC range adjustment. The following procedures assume that a PGA offset adjustment (PGAADJ) subroutine, an ADC offset (ADCOFF) subroutine, and an ADC range (ADCRNG) subroutine similar to those listed in Appendix A are in the resident program.

5-6. PGA OFFSET. The Programmable Gain Amplifier (PGA) provides extremely accurate, software-controlled, amplification of the selected analog input. However, if the PGA is not adjusted properly, significant errors will be introduced when shifting from one gain setting to another. Adjust the PGA as follows:

a. Short input channel 0 by connecting J2 pin 4 to J2 pin 3. (If differential input mode is used, also short J2 pin 6 to J2 pin 4.)

b. Connect high lead of DVM to terminal 61 (figures 5-1 zone C3); connect low lead of DVM to terminal 71 (figure 5-1 zone C2). Set DVM to most-sensitive ac volts scale.

c. Call PGAADJ subroutine and adjust R14 (figure 5-1 zone D5) for minimum DVM indication.

NOTE

If DVM indicates 0V ac while PGAADJ subroutine is running, the PGA is not switching gain properly and corrective action must be taken. (Check the program first.)

5-7. ADC OFFSET. After the PGA offset has been adjusted as described in paragraph 5-6, adjust the ADC offset as follows:

a. Connect precision voltage source to channel 0 as listed in table 5-2.

Table 5-2. ADC Offset and Range Adjustment Test Input

VOLTAGE SOURCE CONNECTION	INPUT MODE	
	SINGLE-ENDED	DIFFERENTIAL
High	J2 pin 4	J2 pin 4
Low	J2 pin 3	J2 pin 6
Ground	J2 pin 3	J2 pin 3

b. Set precision voltage source for appropriate offset input as required for ADC range being used. Refer to table 5-3.

c. Call ADCOFF subroutine and adjust OFFSET trimpot (on edge of ADC module near J3 pin 29) until console readings alternate between the two values listed in 5-4.

Table 5-3. Voltage Source Input Required for ADC Offset and Range Adjustment

ADC RANGE	VOLTAGE SOURCE INPUT	
	OFFSET ADJ	RANGE ADJ
+5V	0.00061V	4.9982V
+10V	0.00122V	9.9963V
±5V	0.00122V	4.9963V
±10V	0.00244V	4.9927V
4-20 mA*	0.00061V	4.9982V

*250-ohm resistors must be installed as described in paragraph 2-17. Voltage source must be capable of supplying 20 mA.

5-8. ADC RANGE. After the PGA offset and ADC offset have been adjusted as described in paragraphs 5-6 and 5-7, adjust the ADC range as follows:

a. Connect precision voltage source to channel 0 as listed in table 5-2.

b. Set precision voltage source for appropriate range input as required for ADC range being used. Refer to table 5-3.

c. Call ADCRNG subroutine and adjust RANGE trimpot (on edge of ADC module near J3 pin 49) until readings alternate between the two values listed in table 5-4.

5-9. SERVICE DIAGRAMS

The SBC 711 parts location diagram and schematic diagram are given in figure 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonics that ends with a slash (e.g., MWTC/) is active low. Conversely, a signal mnemonic without a slash (e.g., EOC) is active high.

5-10. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:
From Alaska or Hawaii call –
(408) 987-8080
From locations within California call toll free –
(800) 672-3507
From all other U.S. locations call toll free –
(800) 538-8014
TWX: 910-338-0026
TELEX: 34-6372

Always contact the MCD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCD Technical Support Center personnel.

NOTE
Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

Table 5-4. ADC Offset and Range Adjustment Readings

ADC CODE*	OFFSET ADJ				RANGE ADJ	
	LOW READING		HIGH READING		LOW READING	HIGH READING
	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR		
Straight Binary	8000	0000	8010	0010	FFE0	FFF0
Offset Binary	0000	8000	0010	8010	7FE0	7FF0

*Refer to paragraph 2-11.

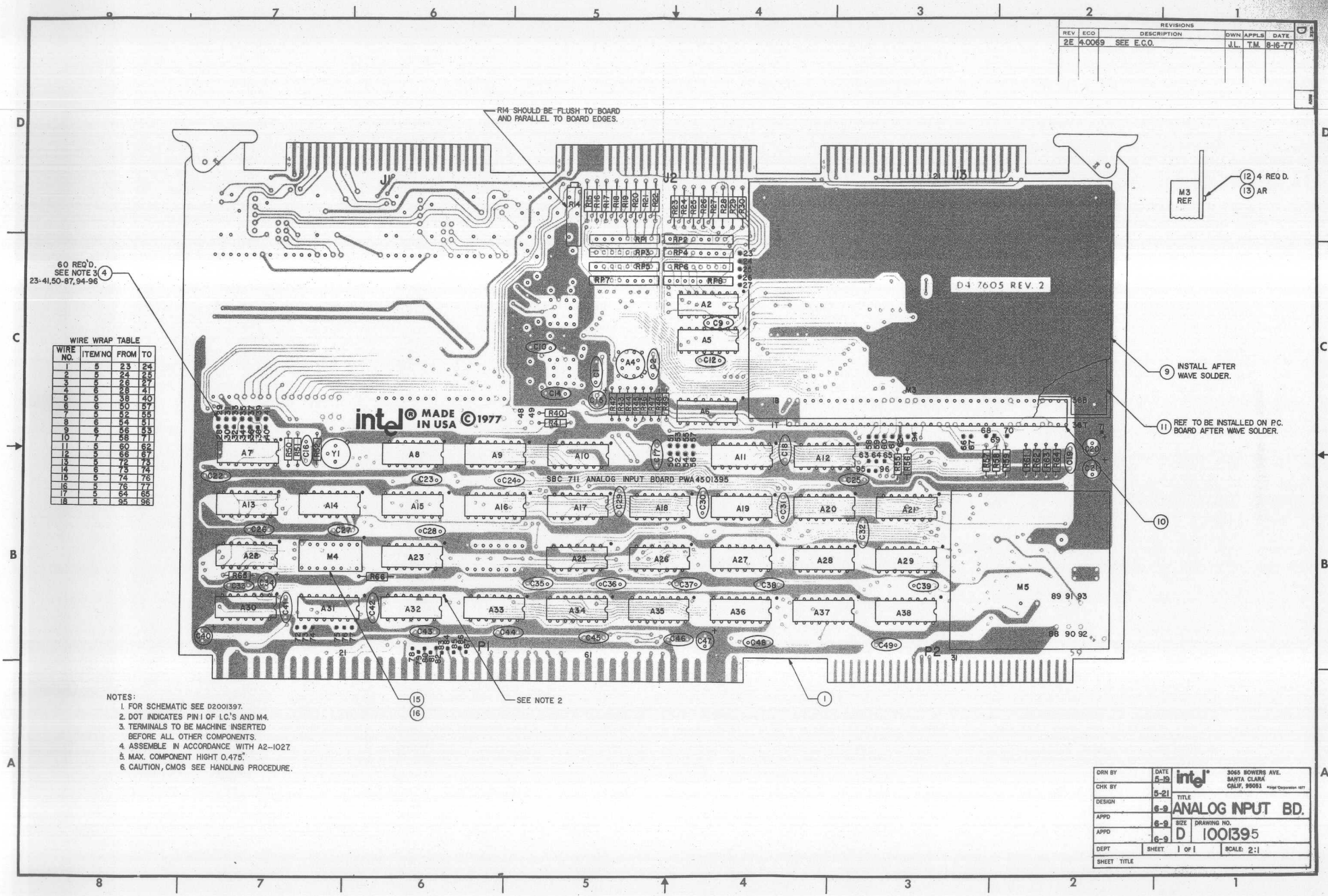
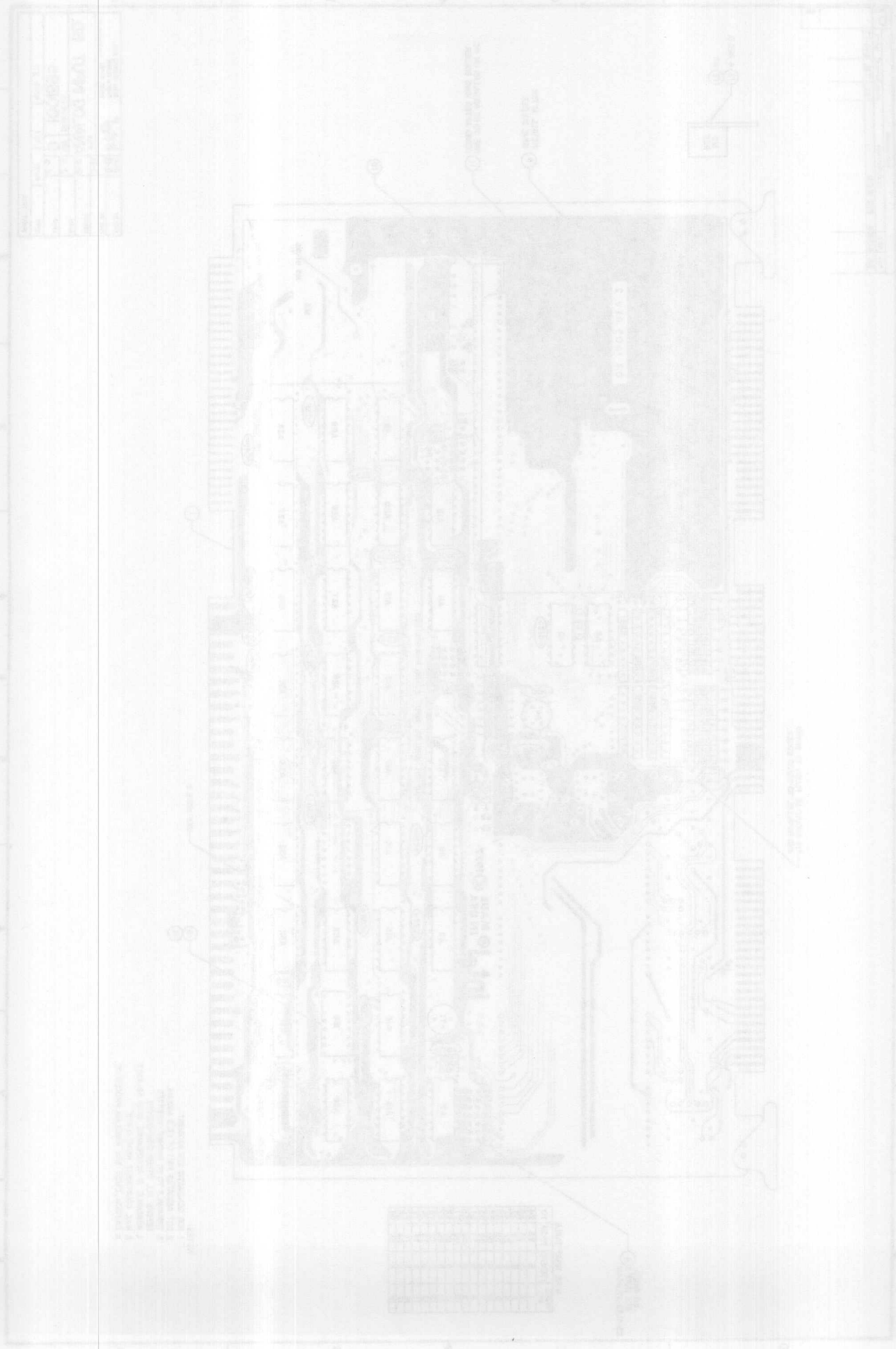


Figure 5-1. SBC 711 Parts Location Diagram



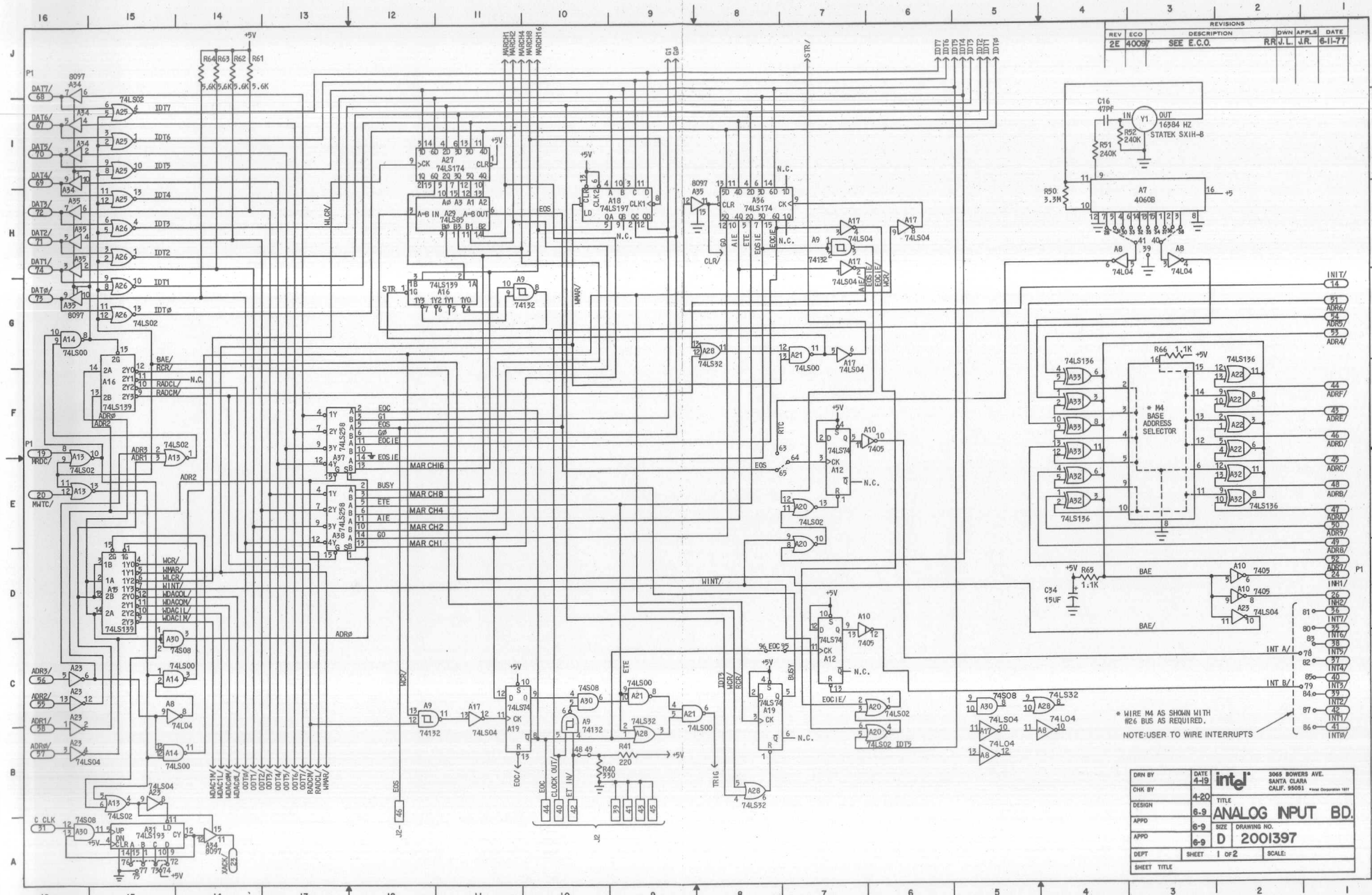


Figure 5-2. SBC 711 Schematic Diagram (Sheet 1 of 2)

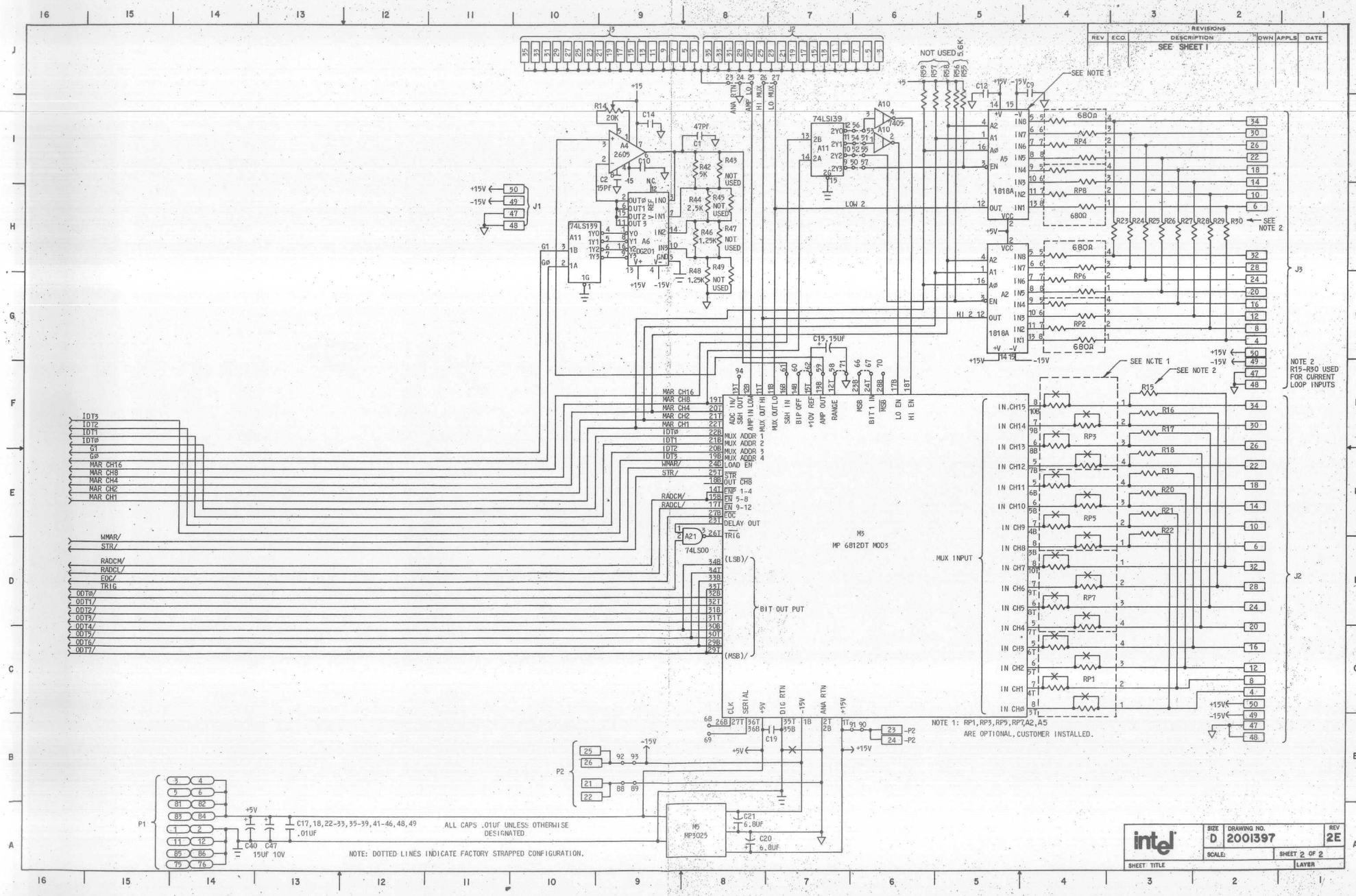


Figure 5-2. SBC 711 Schematic Diagram (Sheet 2 of 2)

APPENDIX A
CALIBRATION PROGRAM

The calibration program presented on this and following pages is required when calibrating the ADC as described in Chapter 5. This program presumes the SBC 711 to be configured for a memory base address of F700 and the console data port and status port to be F6 and F7, respectively.

```
            PUBLIC  PGAADJ  ;PGA ADJUSTMENT.
            PUBLIC  ADCOFF  ;ADC OFFSET ADJUSTMENT.
            PUBLIC  ADCRNG  ;ADC RANGE ADJUSTMENT.

            PUBLIC  RANCHN  ;READ RANDOM CHANNEL.

BASE        EQU     0F700H  ;BASE ADDRESS OF INTERFACE.
SCA         EQU     BASE+0  ;A/D COMMAND REGISTER.
STAT        EQU     BASE+0  ;A/D STATUS REGISTER.
FCR         EQU     BASE+1  ;GAIN, MUX ADDRESS REGISTER.
ADDATA      EQU     BASE+4  ;A/D DATA REGISTER.
GO          EQU     1       ;CONVERSION-ENABLE IN COMMAND REGISTER.
EOC         EQU     80H     ;EOC STATUS.
CHAN0       EQU     0       ;CHANNEL 0.
X1          EQU     0       ;GAIN = 1.
X2          EQU     040H    ;GAIN = 2.
X4          EQU     080H    ;GAIN = 4.
X8          EQU     0C0H    ;GAIN = 8.

CRTD        EQU     0F6H    ;CONSOLE DATA PORT.
CRTS        EQU     0F7H    ;CONSOLE STATUS PORT.
RXRDY       EQU     2       ;RECEIVER READY BIT
TXRDY       EQU     1       ;TRANSMITTER READY BIT.
LF          EQU     0AH     ;ASCII LINE FEED.
CR          EQU     0DH     ;ASCII CARRIAGE RETURN.

;THE FOLLOWING IS A LIST OF ALL PUBLIC VARIABLES USED IN THIS MODULE.
            DSEG
GAIN:       DS      1       ;(0,1,2, OR 3)
FSTCHN:     DS      1       ;(0-31)
LSTCHN:     DS      1       ;(0-31)
DATPTR:     DS      2       ;POINTER TO DATA FIELD.
BUFR:       DS      2       ;BUFFER FOR 'ADCOFF' & 'ADCRNG'.

;*****************************************************************
;SUBROUTINE 'PGAADJ' SWITCHES THE PGA GAIN FROM X1 TO X8 TO
;ALLOW THE USER TO ADJUST THE PGA OFFSET POT (R14) . THE
;PROGRAM WILL RUN UNTIL THE OPERATOR PRESSES A KEY ON THE CONSOLE.

            CSEG
PGAADJ:     LXI     H,FCR   ;POIINT TO GAIN REGISTER.
PGA1:       MVI     M,X1    ;SET GAIN TO X1.
            MVI     M,X8    ;SWITCH TO X8.
            IN      CRTS    ;SEE IF HALT.
            ANI     RXRDY
            JZ      PGA1
            RET

;*****************************************************************
;SUBROUTINES 'ADC0FF' AND 'ADCRNG' CONVERT THE ANALOG INPUT ON
;CHANNEL 0 AND DISPLAY THE RESULT ON THE CONSOLE, FOLLOWED BY A
;CARRIAGE RETURN/LINE FEED. THE DISPLAY IS CONTINUOUSLY UPDATED
;UNTIL THE OPERATOR PRESSES A KEY ON THE CONSOLE TO HALT.

            CSEG
ADCOFF:
ADCRNG:     MVI     A,CHAN0 ;POINT TO CHANNEL 0.
            STA     FSTCHN
```

```
        MVI     A,X1    ;SET GAIN TO X1.
        STA     GAIN

ADC1:   LXI     H,BUFR  ;POINT TO BUFFER.
        SHLD    DATPTR  ;SET BUFFER POINTER FOR 'RANCHN'.
        CALL    RANCHN  ;CONVERT CHANNEL 0 .
        LXI     H,BUFR  ;POIN TO POINTER.
        INX     H       ;POINT TO MSBYTE.
        MOV     C,M     ;LOAD MSBYTE.
        CALL    DBYTE   ;DISPLAY MSBYTE ON CONSOLE.
        DCX     H       ;POINT TO LSBYTE.
        MOV     C,M     ;LOAD LSBYTE.
        CALL    DBYTE   ;DISPLAY LSBYTE ON CONSOLE.

        MVI     C,CR    ;PRINT CR ON CONSOLE.
        CALL    CO
        MVI     C,LF    ;PRINT LINE FEED ON CONSOLE.
        CALL    CO

        IN      CRTS    ;SEE IF OPERATOR WANTS TO HALT.
        ANI     RXRDY
        JZ      ADC1    ;JMP IF OPERATOR CONTINUES.

        RET

;*****************************************************************
;SUBROUTINE RANCHN USES THE GLOBAL VARIABLES 'FSTCHN' AND 'GAIN'
;TO DEFINE THE CHANNEL AND GAIN TO BE USED IN THE CONVERSION
;OF THE ANALOG INPUT. THE RESULT IS STORED AT THE LOCATION
;POINTED BY 'DATPTR'.

        CSEG
RANCHN: LXI     H,FCR   ;POINT HL TO FIRST CHANNEL REGISTER.
        LDA     GAIN    ;LOAD GAIN.
        MOV     C,A
        LDA     FSTCHN  ;LOAD CHANNEL.
        ORA     C       ;ADD GAIN BITS.
        MOV     M,A     ;LOAD FIRST CHANNEL REGISTER.

        DCX     H       ;POINT TO COMMAND/STATUS REGISTER.
        MVI     M,GO    ;START A/D CONVERSION.

RAN1:   MOV     A,M     ;READ STATUS.
        RLC             ;CHECK EOC STATUS.
        JNC     RAN1    ;JMP IF CONVERSION NOT DONE.

        MVI     M,0     ;RESET CONVERSION-ENABLE IN COMMAND REGISTER.
        CALL    LDDATA  ;LOAD CONVERSION DATA INTO DATPTR.

        RET             ;EXIT RANCHN.

;*****************************************************************
;SUBROUTINE 'LDDATA' TAKES THE A/D CONVERTOR DATA AND
;LOADS IT INTO THE MEMORY LOCATIONS POINTED BY 'DATPTR'.

        CSEG
LDDATA: LHLD    ADDATA  ;LOAD CONVERTOR DATA INTO HL.
        XCHG            ;PUT DATA INTO DE.

        LHLD    DATPTR  ;LOAD POINTER TO DATA FIELD.
        MOV     M,E     ;STORE DATA IN MEMORY.
        INX     H
        MOV     M,D
        INX     H
        SHLD    DATPTR  ;SAVE NEW POINTER.
        RET             ;EXIT LADATA.

;*****************************************************************
;SUBROUTINE 'DBYTE' CONVERTS THE BINARY CONTENTS OF REG. C TO
;ASCII AND DISPLAYS THE RESULT ON THE CONSOLE.
```

```
        CSEG
DBYTE:  PUSH    B           ;SAVE REG. C.
        MOV     A,C         ;LOAD DATA.
        RRC                 ;SWAP LOW NIBBLE
        RRC                 ;WITH HIGH NIBBLE.
        RRC
        RRC
        MOV     C,A
        CALL    HXASC       ;CONVERT HIGH NIBBLE TO ASCII.
        MOV     C,A
        CALL    CO          ;DISPLAY RESULT ON CONSOLE.
        POP     B           ;LOAD EXTRA COPY OF DATA.
        CALL    HXASC       ;CONVERT LOW NIBBLE TO ASCII.
        MOV     C,A
        CALL    CO          ;DISPLAY LOW NIBBLE ON CONSOLE.
        RET                 ;EXIT DBYTE.

;*************************************************************
;SUBROUTINE 'HXASC' CONVERTS THE LOW NIBBLE OF REG. C INTO
;ITS ASCII EQUIVALENT. RESULT RETURNED IN REG. A.

        CSEG
HXASC:  MOV     A,C         ;LOAD DATA.
        ANI     0FH         ;CLEAR HIGH NIBBLE.
        CPI     10          ;SEE IF < 9.
        JC      HX1         ;JMP IF < 9.
        ADI     7           ;CORRECT FOR A-F.
HX1:    ADI     '0'         ;ADD ASCII ZONE.
        RET                 ;EXIT HXASC.

;*************************************************************
;SUBROUTINE 'CO' DISPLAYS THE CONTENTS OF REG. C ON THE CONSOLE.

        CSEG
CO:     IN      CRTS        ;SEE IF TRANSMITTER IS READY.
        ANI     TXRDY
        JZ      CO          ;JMP IF NOT READY.
        MOV     A,C         ;LOAD OUTPUT DATA.
        OUT     CRTD        ;DISPLAY DATA ON CONSOLE.
        RET                 ;EXIT CO.
        END
```